System Engineering Notes
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Differences between the SYM53C720 and the SYM53C8XX Family
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This SCSI engineering note compares the main features and functions of the SYM53C720 to all members of the SYM53C8XX family of PCI-SCSI I/O Processors. It also lists the bit, register, and pin differences between all of these devices. For additional information, refer to the appropriate product data manual.

Features Summary

The SYM53C720 and the SYM53C8XX family of SCSI I/O Processors are based on the same architecture, and share many common features. They transfer data at 5 MB/s asynchronous and 10 MB/s synchronous for 8-bit SCSI; the devices that support 16-bit SCSI transfer data at 10 MB/s asynchronous or 20 MB/s synchronous. All of the devices can be programmed with SCSI SCRIPTS, which allows easy firmware upgrades to maintain compatibility with current and future SCSI standards, as well as customized applications. Both product families are SCRIPTS-compatible. Both families also provide Symbios Logic TolerANT SCSI driver and receiver technology, to assure reliable operation in all cabling environments.

SYM53C720

The SYM53C720 can be interfaced to both Motorola and Intel-based host processors, and supports both Big and Little Endian byte ordering, for a total of seven different host bus interface modes. In addition to allowing faster SCSI data transfers, wide SCSI allows up to 16 devices on the SCSI bus, and supports the Chained Block Move instruction for handling odd-aligned wide transfers. The SYM53C720 supports both single-ended and differential transfers, and has a DMA transfer rate of 105 MB/s. It is packaged in a 208 pin quad flat pack.

SYM53C810

In the SYM53C810, the multiple host bus interfaces of the SYM53C720 were replaced by a direct interface to the PCI bus. These devices are optimized for placement directly on the motherboard. The SYM53C8XX are full 32-bit, zero wait state PCI DMA bus masters with a burst rate of 110 MB/s (@ 33MHz).

The SYM53C810 operates in single-ended mode only, and supports the 8-bit (non-wide) SCSI bus. The SYM53C810 is packaged in a 100 pin PQFP.

SYM53C815/53C825

The SYM53C815 and SYM53C825 are ideal for motherboard or host adapter implementation in personal computers and workstations. They are based on the SYM53C810 and SYM53C820, with the addition of the new features described in this section. These chips have an additional port for a BIOS PROM for complete add-in board support. This external memory interface allows the system designer to store the BIOS in EPROM or FLASH memory without impacting the size of the system BIOS. The devices support up to 1 MB of external ROM in binary increments starting at 16 KB. For easy software development, the external memory interface supports local programming of flash memory. The size and speed of the external memory is configured by pull-down resistors at power up.

To optimize bus utilization, the SYM53C815 and SYM53C825 burst fetch the first two longwords of all instructions when the Burst Op Code Fetch bit is set in the DMODE register. In Memory-to-Memory Moves and indirect instruction types, an additional longword is also fetched in a second bus ownership. A table indirect move instruction causes two burst fetches of two longwords each, for a total of four longwords in two bus ownerships.

The SYM53C815/SYM53C825 support both Big and Little Endian byte addressing for SCSI data and external memory accesses. In Big Endian mode, the first byte of an aligned SCSI to PCI transfer is routed to byte lane three and succeeding transfers are routed to lanes two, one, and zero. The difference between these two devices is that the SYM53C815 supports 8-bit SCSI transfers in single-ended mode only, and the SYM53C825 supports both 8-bit and 16-bit transfers in either single-ended or differential mode. The SYM53C815 is packaged in a 128-pin PQFP. The SYM53C825 is packaged in a 160 pin PQFP.

The SYM53C815 uses additional pins to reduce the number of external components required to implement the external ROM interface logic, allowing a lower cost solution than the SYM53C825.

Burst Transfers

The SYM53C720 and the SYM53C8XX family can all burst data, but they perform bursts in different ways. The SYM53C720 can transfer up to 16 longwords in a single bus ownership with cache line bursting. With this method, the data being transferred is sent four longwords at a time along with an address. The SYM53C8XX family performs PCI bursts of 2, 4, 8, or 16 longwords with only one longword of address information. For example, to burst 16 longwords of data the SYM53C720 would send one longword of address information and four longwords of data, and repeat the operation four times. The SYM53C8XX would send one longword of address information followed by 16 longwords of data.

Packaged Software Support

Symbios Logic offers a total SCSI solution for the SYM53C810, SYM53C815, and SYM53C825 with the SCSI Device Management System, a complete software package that includes BIOS and drivers to support most types of SCSI peripherals for the major PC-based operating systems.

Bit and Register Differences

	SYM 53C720	SYM 53C810	SYM 53C815	SYM 53C825
SCNTL0 Register				
Bit 2, Enable Parity Generation	yes	no	no	no
SCNTL2 Register				
Bit 6, Chained Mode	yes	no	no	yes
Bit 3, Wide SCSI Send	yes	no	no	yes
Bit 0, Wide SCSI Receive	yes	no	no	yes
SCNTL 3 Register				
Bit 3, Enable Wide SCSI	yes	no	no	yes
GPREG Register				
Bits 4-2, General Purpose I/O 2-4	yes	no	yes	yes
DSTAT Register				
Bit 6, Master Data parity Error	no	yes	yes	yes
Bit 6, Host Parity Error	yes	no	no	no
Bit 1, Watchdog Time-out Interrupt Detected	yes	no	no	no
SSTAT2 Register				
Bit 7 SIDL Most Significant Byte Full	yes	no	no	yes
Bit 6, SODL Most Significant Byte Full	yes	no	no	yes
Bit 5, SODL Most Significant Byte Full	yes	no	no	yes
Bit 3, Latched SCSI Parity for SD 15-8	yes	no	no	yes
Bit 0, SCSI SDP1 Signal	yes	no	no	yes
CTEST0 Register				
Bit 7, Cache Burst Disable	yes	no	no	no

	SYM 53C720	SYM 53C810	SYM 53C815	SYM 53C825
Bits 6-5, Snoop Control	yes	no	no	no
Bit 4, Generate Receive Parity for Pass-Through	yes	no	no	no
Bit 3, DMA FIFO Parity	yes	no	no	no
Bit 2, Even Parity	yes	no	no	no
Bit 1, Transfer Type Bit 1	yes	no	no	no
Bit 0, Cache 386 Enable	yes	no	no	no
CTEST2 Register				
Bit 5, Configured as I/O	no	yes	yes	yes
Bit 4, Configured as Memory	no	yes	yes	yes
Bit 3, DMA FIFO Parity Bit	yes	no	no	no
CTEST3 Register				
Bit 0, Snoop Pin	yes	no	no	no
CTEST4 Register				
Bit 7, Host Bus Multiplex	yes	no	no	no
Bit 7, Burst Disable	no	yes	yes	yes
Bit 3, Host Parity Check Enable	yes	no	no	no
Bit 3, Master Parity Error Enable	no	yes	yes	yes
DMODE Register				
Bit 5-4, Function Code Bits 1-0	yes	no	no	no
Bit 5, Source I/O-Memory Enable	no	yes	yes	yes
Bit 4, Destination I/O-Memory enable	no	yes	yes	yes
Bit 3, Program Data	yes	no	no	no
Bit 3, Enable Read Line	no	yes	yes	yes
Bit 2, Fixed Address Mode	yes	no	no	no
Bit 1, Burst Op Code Fetch Enable	no	no	yes	yes
DIEN Register				
Bit 6, Host Parity Error Detected	yes	no	no	no
Bit 6, Master Data Parity Error	no	yes	yes	yes
Bit 1, Enable Watchdog Time-out Interrupt	yes	no	no	no

	SYM 53C720	SYM 53C810	SYM 53C815	SYM 53C825
DCNTL Register				
Bits 7, Size Throttle Enable	yes	no	no	no
Bit 6, Bus Mode	yes	no	no	no
Bit 5, Enable ACK	yes	no	no	no
Bit 3, IRQ Mode	no	yes	yes	yes
Bit 3, Host Bus Width Equal to 16	yes	no	no	no
Bit 1, Fast Arbitration	yes	no	no	no
SWIDE Register	yes	no	no	yes
GPCNTL Register				
Bit 7, Master Enable	no	yes	yes	yes
Bit 6, Fetch Enable	no	yes	yes	yes
Bits 4-3, GPIO4-3 Enable	yes	no	yes	yes
RESPID1 Register	yes	no	no	yes
STEST1 Register				
Bit 7, SCLK	no	yes	yes	yes
Bits 1-0, SCSI FIFO Parity Bits 1-0	yes	no	no	no
STEST2 Register				
Bit 5, SCSI Differential Mode	yes	no	no	yes
Bit 2, Always Wide SCSI	yes	no	no	yes

SCRIPTS Instruction Differences

The SYM53C720 and the SYM53C8XX family use the same SCRIPTS instruction set, for easy migration of software between products. The only difference is the Chained Move instruction, which is only available on devices that support wide SCSI. This instruction is not available in the SYM53C810 or SYM53C815.

Pin Differences

The differences in the pin configuration among the SYM53C720 and the SYM53C8XX family can be grouped into several general areas. Since the SYM53C720 supports a variety of host bus interfaces, these pins differ significantly from the host interface pins for the PCI-compatible devices. The SYM53C810 and SYM53C815 do not support wide SCSI or differential operation, so the pins needed to support these features are unavailable on these two devices. Finally, the SYM53C815 and SYM53C825 contain additional pins to support the local external memory interface for dedicated add-on ROM. The pin differences are summarized in the following table.

	SYM 53C720	**SYM 53C810**	**SYM 53C815**	**SYM 53C825**
Bus Mode Select Pins	yes	no	no	no
Differential Sense	yes	no	no	yes
Differential Support Lines	yes	no	no	yes
Big/Little Endian Select	yes	no	yes	yes
General Purpose Input/Output 3-4	yes	no	yes	yes
General Purpose Input/Output 2_Memory Address Strobe 2	no	no	yes	yes
General Purpose Input/Output 2	yes	no	no	no
Memory Address Strobe 1	no	no	yes	yes
Memory Address Strobe 0	no	no	no	yes
Memory Address/Data Bus 7-0	no	no	yes	yes
Memory Address Bus 7-0	no	no	yes	no
Memory Write Enable	no	no	yes	yes
Memory Output Enable	no	no	yes	yes
Memory Chip Enable	no	no	yes	yes

Configuration Space Differences

The PCI Configuration Space is available only in the SYM53C8XX family of PCI-SCSI Processors. One difference in this space within the SYM53C8XX family is the Expansion ROM Base Address Register, which is available only in the SYM53C815 and SYM53C825. In addition, each device has a different value in the Device ID register, which is located at Address 02h in the configuration space. For more information on the PCI configuration space, refer to the *PCI Specification* or the SYM53C8XX family data manuals.