SYMBIOS LOGIC

System Engineering Notes

No. 849
SYM53C720 to VESA Local Bus Interface
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This application note defines a logical interface between the SYM53C720 and the VESA Local Bus (VL-Bus). It contains guidelines for designing systems that use the SYM53C720/VL-Bus interface. This application note concentrates only on interfacing the SYM53C720 to the VL-Bus. Information on interfacing the SYM53C720 to the SCSI bus can be found in SYMSCSI Engineering Notes 833 or 836. The pound symbol (#) is used with Intel signal names to indicate that the active state occurs when the signal is at a low voltage; active low signals in the SYM53C720 are indicated by a slash (/) following the signal name.

NOTE: this interface has not been tested, so the designer should perform a thorough design analysis before implementing this interface.

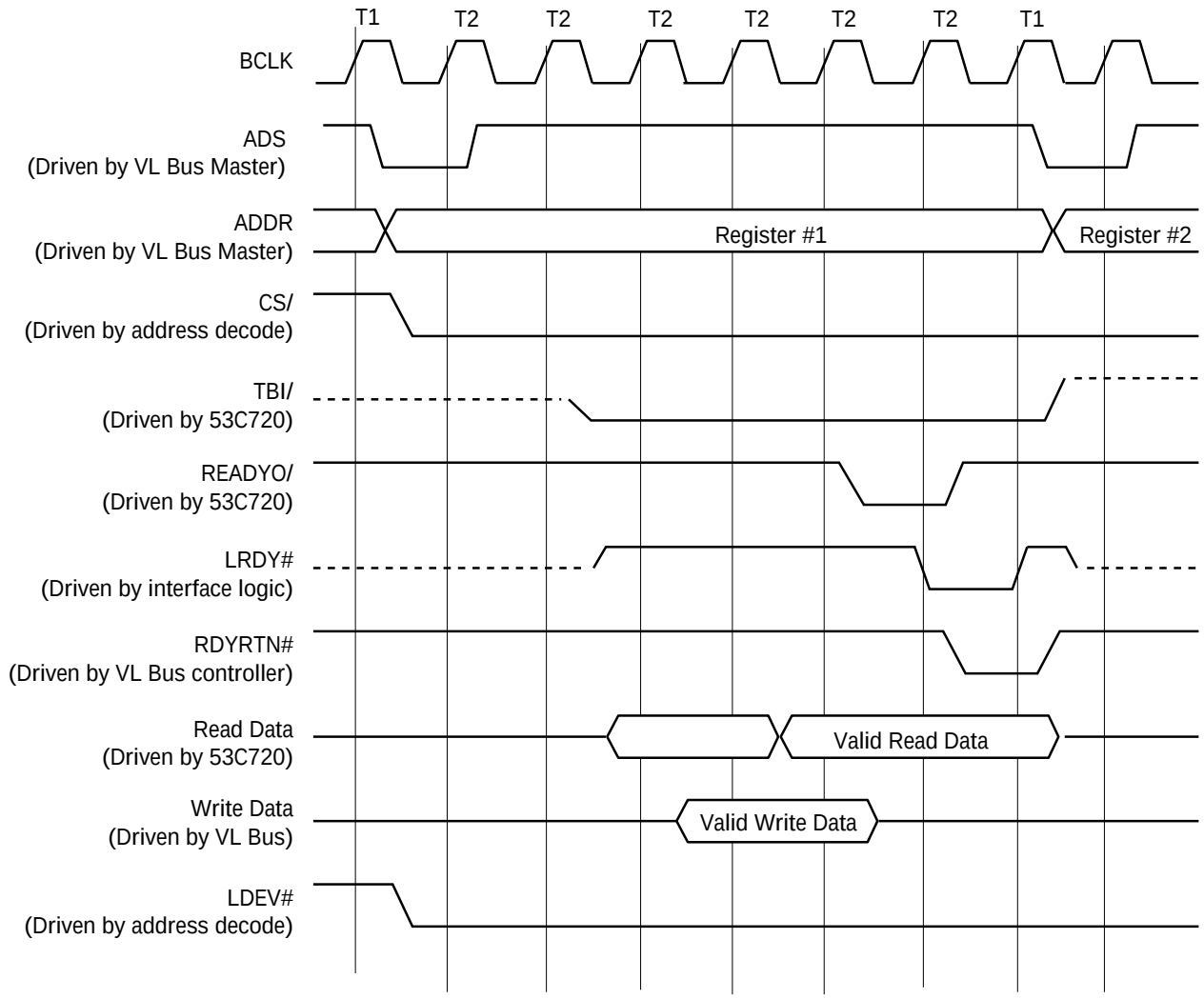
Host Interface

The SYM53C720 bus mode pins (BS(2-0)) are all tied to ground, enabling the chip to operate in Bus Mode 4, 80386 Little Endian mode. Two signals from the 53C720, HOLD/ and MASTER/, are ANDed to generate the VL-Bus Local Request signal, LREQ#. Since bus retries are not allowed on the VL-Bus, the SYM53C720 TEA/ pin should tied to V_{DD} through a 1 KΩ resistor. Because of the arbitration protocol of the VL-Bus, the SYM53C720 BOFF/ pin should be tied to V_{DD} through a 1KΩ resistor. If the SYM53C720 BB/ pin is not used, it should be tied to V_{DD} through a 1 KΩ resistor so the SYM53C720 will operate properly during bus arbitration.

Slave Cycles

A VL-Bus Master performs a slave read/write access to the SYM53C720 using a five-wait state cycle. System logic must perform the address decode for the SYM53C720 and select the chip by asserting the Chip Select (CS/) signal. CS/ must meet timings t_3 and t_4 (CS/ setup to and hold from BCLK high after ADS/) specified in the Bus Mode 4 Slave Read/Write Cycle section in Chapter Six of the SYM53C720 *Data Manual*. The address decode logic should also return the LDEV# (VL-Bus Target Local Device) signal to the VL-Bus Controller. Therefore, CS/ and LDEV# can be the same signal. The interface logic will generate the LRDY# (VL-Bus Local Ready) signal. The LRDY# signal is a one-clock delayed version of the SYM53C720 READYO/ (Ready Out) signal. For the SYM53C720 to terminate the slave access, the VL-Bus Controller must generate a RDYRTN# (Ready Return) that will be sampled by the chip. For a slave read access, the SYM53C720 will hold the read data until RDYRTN# is sampled active. The VL Bus BLAST# signal can be ignored, since the chip cannot burst during slave accesses. See the Slave Cycle waveforms in Figure 1 and the SYM53C720 *Data Manual* for more information.

Figure 1. SYM53C720 and VL-Bus Slave Cycle



Master Cycles

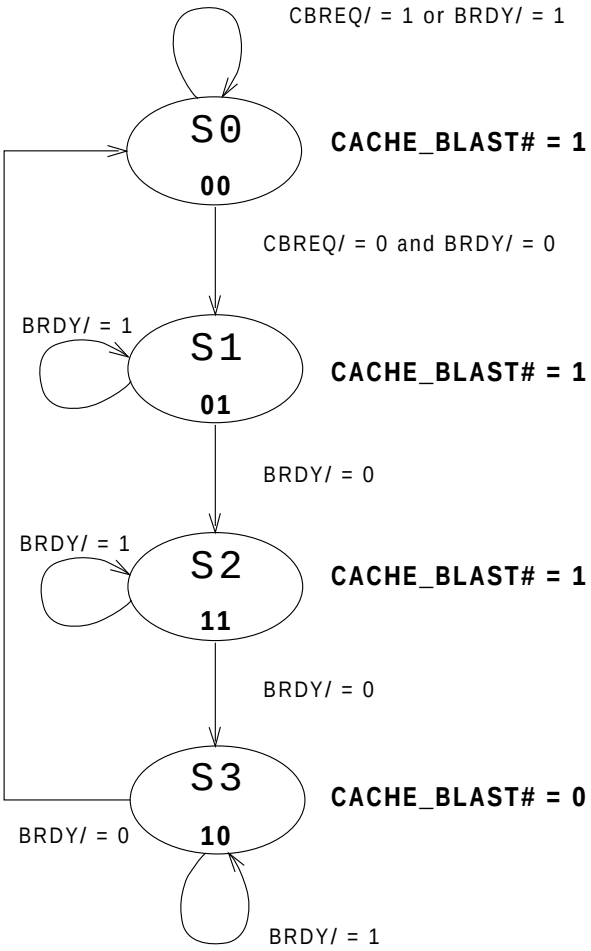
The interface logic must generate the BLAST# signal, to indicate to the memory system that the next time LRDY# (VL-Bus Controller generates RDYRTN#) or BRDY# is returned, the data cycle transfer will terminate. The interface logic should generate two burst last signals, then logically AND to generate the system BLAST# signal. The first burst last signal, NON_CACHE_BLAST#, will be for the basic two-clock data cycle. This signal is implemented using a clocked J-K flip-flop. The J, K and NON_CACHE_BLAST# equations are as follows:

```
J = ! ( ! CBREQ/ + ADS/ + MASTER/)

K = ! RDYRTN#

NON_CACHE_BLAST# = ! Q
```

The signals CBREQ/, ADS/ and MASTER/ are outputs from the SYM53C720. The signal RDYRTN# is an output from the VL-Bus Controller and is generated from the LRDY# output by the memory system.

For the SYM53C720 to perform cache line bursts as illustrated in the SYM53C720 *Data Manual*, in register CTEST0, bit 0 (C386E) must be set and bit 7 (CDIS) must be cleared. The second burst last signal, CACHE_BLAST#, is generated by implementing a four-state grey code state machine with the state diagram in Figure 2.

Figure 2. State Diagram



The next state equations for the state machine are given below. Qb is the most significant bit.

```
Qb(n+1) = ((Qa & ! BRDY#) + (Qb & BRDY#))
Qa(n+1) = ((Qa & BRDY#) + (! Qb & Qa) + (! Qb & ! CBREQ/ & ! BRDY#))
```

The output equation for CACHE_BLAST# is given below. This signal will not glitch during state transition since a grey code was used for state encoding.

```
CACHE_BLAST# = ! (Qb & ! Qa)
```

Logically ANDing NON_CACHE_BLAST# and CACHE_BLAST# will give the signal needed to drive the system BLAST# to the memory system.

```
BLAST# = NON_CACHE_BLAST# & CACHE_BLAST#
```

For the SYM53C720 to transfer data on the VL-Bus, two more signals must be discussed. The first is the SYM53C720 READYI/ input signal. RDYRTN# and BRDY# should be logically ANDed to generate the SYM53C720 READYI/ signal. The system RDYRTN# should be connected to the SYM53C720 TBI/ signal, since the memory system will return LRDY# for non-burst data transfers. This will indicate to the 53C720 that the data cycle is not a cache line burst and the SYM53C720 will resume with the basic two-clock data cycle. If the memory system does not perform bursts, it must return LRDY# during the first data transfer. Returning LRDY# during the second, third or fourth data transfer of a SYM53C720 cache line burst could result in improper operation of the chip. See the section "Bus Mode 4 Bus Master Read/Write (Cache Line Burst)" in Chapter Six of the SYM53C720 *Data Manual*, for proper operation.

The designer may choose the type of circuit components used to implement the above logic. Figure 3 illustrates the signal activity on the SYM53C720 during master cycles. Figure 4 is an interface diagram that shows the logical connections between the SYM53C720 and the VL-bus.

Figure 3. SYM53C720 Master Cycle

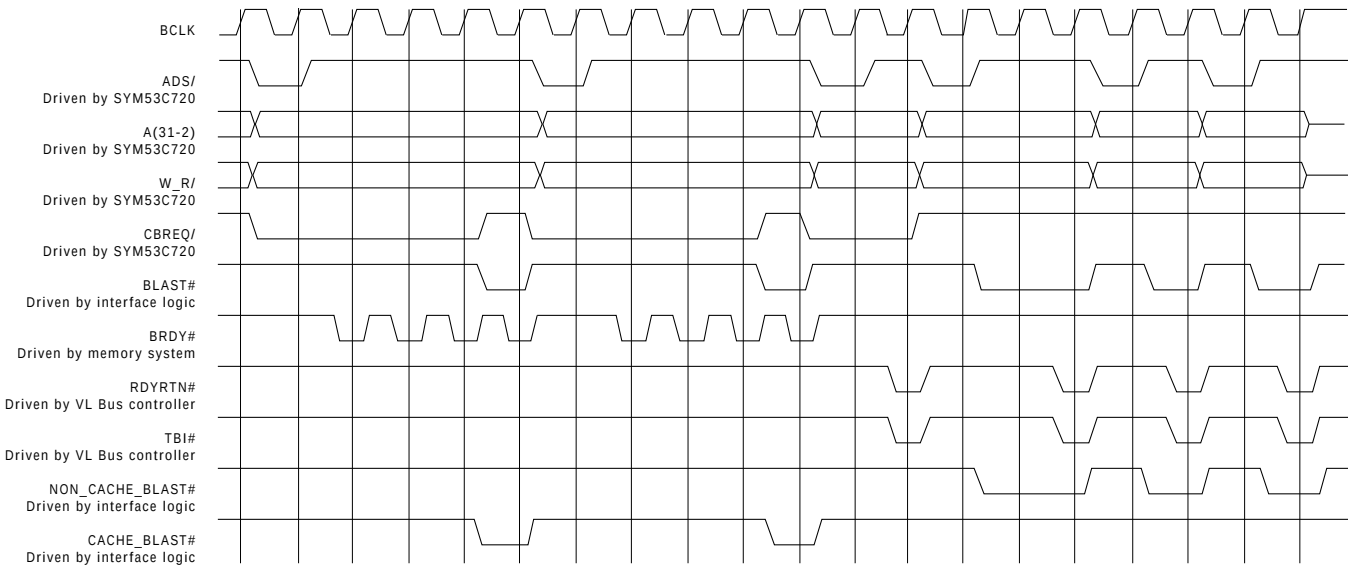


Figure 4. SYM53C720/VL Bus Interface Diagram