SYMBIOS LOGIC

System Engineering Notes

No. 848
SYM53C720 to 80486 Interface
Rev. 1.0 , 2/93

This application note defines a logical interface between the SYM53C720 and the Intel 80486 microprocessor. It contains guidelines for designing systems that use the SYM53C720/80486 interface. This application note concentrates only on interfacing the SYM53C720 to the 80486 local bus. Information on interfacing the SYM53C720 to the SCSI bus can be acquired from SCSI Engineering Notes 833 or 836. The pound symbol (#) is used with Intel signal names to indicate the active state occurs when the signal is at a low voltage; active low signals in the SYM53C720 are indicated by a slash (/) following the signal name.

NOTE: this interface has not been tested and the designer should perform a thorough design analysis before implementing this interface.

Host Interface

The SYM53C720 bus mode pins (BS(2-0)) are all tied to ground, enabling the chip to operate in Bus Mode 4, 80386 Little Endian mode; this bus mode should be used for interfacing with the 80486. The RESET signal must be inverted before being presented to the SYM53C720. Two signals from the SYM53C720, HOLD/ and MASTER/, are NANDed to generate the 80486 Bus Hold Request input, HOLD. The 80486 hold acknowledge signal, HLDA, must be inverted before connecting to the SYM53C720 HLDAI/ pin. Since bus retries are not allowed on the 80486 local bus, the SYM53C720 TEA/ pin should tied to V_{DD} through a 1 KΩ resistor. If the SYM53C720 BB/ pin is not used, it should be tied to V_{DD} through a 1 KΩ resistor, so the SYM53C720 will operate properly during bus arbitration.

Slave cycles

The 80486 performs a slave read/write access to the SYM53C720 using a four wait state cycle. System logic must perform the address decode for the SYM53C720 and select the chip by asserting the Chip Select (CS/) signal. CS/ must meet timings t_3 and t_4 (CS/ setup to and hold from BCLK high after ADS/) specified in the Bus Mode 4 Slave Read/Write Cycle section in Chapter Six of the SYM53C720 *Data Manual*. The first 80486 access to the SYM53C720 should set the EA bit (bit 5) in the DCNTL register. Setting the EA bit will cause the READYI/ pin to become bi-directional; in other words, the SYM53C720 will generate READYI/ during slave accesses. This signal will be connected to the 80486 RDY# signal, indicating that a burst cycle to the SYM53C720 cannot be performed. If the designer decides not to set the EA bit in DCNTL, then system logic must monitor the SYM53C720 READYO/ signal in order to generate READYI/ to the SYM53C720 and RDY# to the 80486. The 80486 BLAST# signal can be ignored, since the 53C720 cannot burst during slave accesses.

Master cycles

The interface logic must generate the BLAST# signal, to indicate to the memory system that the next time RDY# or BRDY# is returned, the data cycle transfer will terminate. The interface logic should generate two burst last signals then logically AND to generate the system BLAST# signal. The first burst last signal, NON_CACHE_BLAST#, will be for the basic two clock data cycle. This signal is implemented using a clocked J-K flip-flop. The J, K and NON_CACHE_BLAST# equations are as follows:

```
J = ! ( ! CBREQ/ + ADS/ + MASTER/)

K = ! RDY#

NON_CACHE_BLAST# = ! Q
```

The signals CBREQ/, ADS/ and MASTER/ are outputs from the 53C720. The signal RDY# is an output from the memory system.

For the SYM53C720 to perform cache line bursts as illustrated in the SYM53C720 *Data Manual*, in register CTEST0, bit 0 (C386E) must be set and bit 7 (CDIS) must be cleared. The second burst last signal, CACHE_BLAST#, is generated by implementing a four-state grey code state machine with the state diagram in Figure 1.

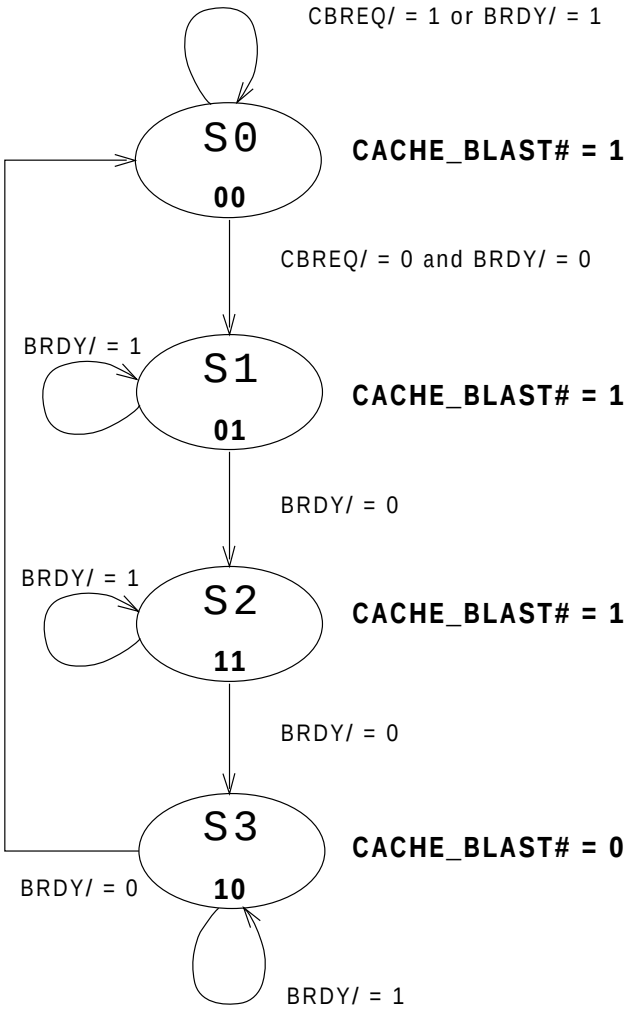

Figure 1. State Diagram

The next state equations for the state machine are given below. Qb is the most significant bit.

```
Qb(n+1) = ((Qa & ! BRDY#) + (Qb & BRDY#))

Qa(n+1) = ((Qa & BRDY#) + (! Qb & Qa) + (! Qb & ! CBREQ/ & ! BRDY#))
```

The output equation for CACHE_BLAST# is given below. This signal will not glitch during state transition, since a grey code was used for state encoding.

```
CACHE_BLAST# = ! (Qb & ! Qa)
```

Logically ANDing NON_CACHE_BLAST# and CACHE_BLAST# will give the signal needed to drive the system BLAST# to the memory system.

```
BLAST# = NON_CACHE_BLAST# & CACHE_BLAST#
```

In order for the SYM53C720 to transfer data on the 80486 local bus, two more signals must be discussed. The first is the READYI/ input signal. Both the system RDY# and BRDY# should be logically ANDed to generate the READYI/ signal for the SYM53C720. The system RDY# should be connected to the SYM53C720 TBI/ signal since the memory system will return RDY# for non-burst data transfers. This will indicate to the SYM53C720 that the data cycle is not a cache line burst and the SYM53C720 will resume with the basic two clock data cycle. If the memory system does not perform bursts, it must return RDY# to the SYM53C720 during the first data transfer. Returning RDY# during the second, third or fourth data transfer of a SYM53C720 cache line burst could result in improper operation of the SYM53C720. See the Bus Mode 4, Bus Master Read/Write (Cache Line Burst) timings in Chapter Six of the SYM53C720 *Data Manual* for proper operation.

The designer may choose the type of circuit components used to implement the above logic. Figure 2 illustrates signal activity on the SYM53C720 during master cycles. Figure 3 is an interface diagram that shows the logical connections between the SYM53C720 and the 80486 processor.

Figure 2. SYM53C720 Master Cycle

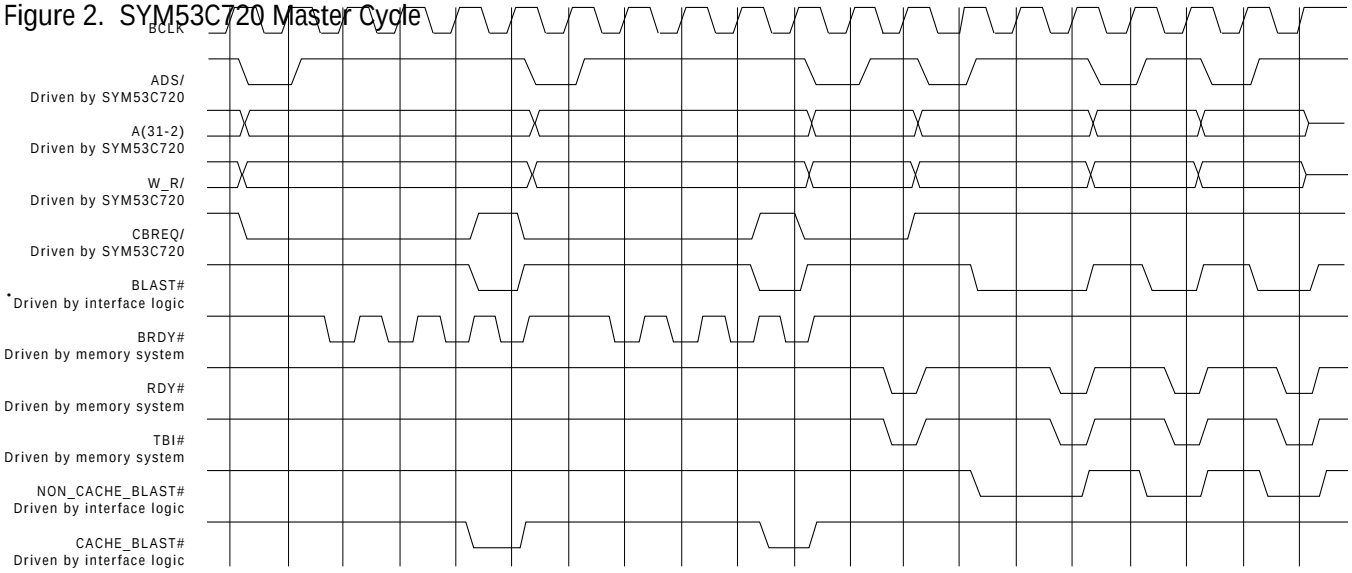

Figure 4. SYM53C720 to 80486 Interface