System Engineering Notes
No. 837
SYM53C710/20 BERR/_TEA/ Pin Function
Rev 2.0, May 1997

Introduction

This engineering note describes the function of the BERR/_TEA/ pin on the SYM53C710/20 SCSI I/O processor. It applies to the following part numbers: 609-3400527, 609-3400654 and 609-3400669.

Functionality of BERR/_TEA/ during Bus Master Mode

In Bus Master Mode, BERR/_TEA/ is used in conjunction with TA/ to indicate to the SYM53C710/20 that one of the following conditions has occurred:

SYM53C710 or SYM53C720 in bus modes 1, 2, 3, or 4

TEA	TA/	CONDITION
1	1	Execute a Wait State
1	0	Normal Cycle Acknowledge
0	1	Bus Error Condition Has Occurred
0	0	Retry the Current Cycle After Relinquishing the Bus *

* In 040 Mode the chip will attempt a bus retry operation if TEA/ is asserted in conjunction with TA/.
* In 030 Mode the chip will attempt a bus retry operation only if BERR/ is asserted in conjunction with HALT/.

Functionality of BERR/_TEA/ during Slave Mode

In Slave Mode the SYM53C710/20 will respond to requests from an external master in one of the following ways:

SYM53C710

TEA/	SLACK/	TA/*	CONDITION
1	1	1	Requests the Bus Master to Insert a Wait State
1	0	0	Normal Cycle Acknowledge
0	1	1	Access Exception Has Occurred
0	0	0	Will not occur

* TA/ Will not be asserted during slave cycles unless the Enable Ack bit in the DCNTL register is set.

Address exceptions are as follows:

040 Mode:	any misaligned 2-byte transfer (A0 = 1) any misaligned longword (A1-A0 not equal to 00) any 2-byte transfer in Big Endian mode
030 Mode:	All of the cases mentioned above plus any 3-byte transfer

SYM53C720

TEA/	SLACK/	TA/*	CONDITION
1	1	1	Requests the Bus Master to Insert a Wait State
1	0	0	Normal Cycle Acknowledge
0	1	1	Access Exception Has Occurred
0	0	0	Will not occur

* TA/ will not be asserted during slave cycles unless the Enable Ack bit in the DCNTL register is set.

Address exceptions are as follows:

040 Mode:	any misaligned 2-byte transfer (A0 = 1) any misaligned longword (A1-A0 not equal to 00) any 2-byte transfer in Big Endian mode
030 Mode:	All of the cases mentioned above plus any 3 byte transfer.
386SX/DX Mode:	No bus exceptions will occur and the TEA/ pin will never be asserted. One, Two, Three, and Four byte operations are allowed.