System Engineering Notes

No. 836
SYM53C720 to 80386SX Interface
Rev. 2.0, August 1993

This application note provides a suggested interface between the SYM53C720 and the Intel 80386SX. The purpose of this application note is to guide people in their own designs. Please note that the interface has not been tested, and the designer should perform a thorough design analysis before implementing this interface.

Host Interface

The interface to the Intel 80386SX host processor, requires the SYM53C720 to operate in Bus Mode 3, the 80386SX little endian mode. To select this mode, tie the SYM53C720 Bus Mode Select pin BS0 high through a 10 KΩ resistor and tie BS2-BS1 to ground. For more information on the host bus modes supported by the SYM53C720, refer to the *SYM53C720 Data Manual*.

The SYM53C720 – Intel 80386SX interface is illustrated in Figure 1. It uses an MC88915, a low skew CMOS PLL clock driver, to multiply the input clock by two. This 2x clock output drives the Intel 80386SX. The four General Purpose Input pins of the SYM53C720 are connected to jumpers so that the chip ID can be read in during boot up. The SYM53C720 SCRIPTS Autostart pin is tied low so the SYM53C720 will automatically fetch and execute SCRIPTS at power-up. The SCSI clock is connected to a 50 MHz oscillator so the SYM53C720 can support fast SCSI. TEA/ (Transfer Error Acknowledge) and TBI/ (Transfer Burst Inhibit) are tied resistively high and low through a 10KΩ resistor respectively. Bus retries and cache bursts cannot be performed.

When interfacing the SYM53C720 to the 80386SX, the following lines should be pulled high with resistors:

SYM53C720	80386SX
A31-A24, PA/, DP3_ABRT/, BB/, BOFF/, BS0/, TEA/, DP2-0, AUTO/, DS_DLE/	NA/, LOCK/

These lines should be tied to ground:

SYM53C720	80386SX
BS2, BS1	n/a

The SYM53C720 Transfer Burst Inhibit pin should be tied low with resistors.

PALs

The interface employs two pals. Their logical functions are described below.

Address decode logic: A PAL (22V10) is used to decode the SYM53C720 addresses and select the chip by asserting the Chip Select (CS/) signal. The address selecting the chip is D000 0XXX hex. This address is defined as the cartridge ROM area in the AT system memory map. Please refer to the attached ABEL listing.

80386SX/SYM53C720 glue logic: A PAL (16V8) is used to generate the Intel Hold and the Memory-I/O signals. In addition, the SYM53C720 Hold Acknowledge and Reset signals are inverted. Please refer to the attached ABEL listing.

Tie bi-directional tri-state outputs high through 10 KΩ pull-up resistors if there is a possibility that these signals will temporarily leave an input in the high impedance state. Unused input signals must be held at a valid logic level. In this circuit, all unused inputs are tied high to minimize current draw.

The SYM53C720 has separate ground planes within the internal logic and the output drivers. Decoupling capacitors are recommended for optimum noise isolation. Use 0.l μF decoupling capacitors between the following ground and power pins on the SYM53C720:

V_{SS} Ground Pin	V_{DD} Power Pin
3	204
16	13
22	27
44	56
71	66
87	82
100	97
119	122
190	186

The upper 16 data lines (D31-16) and the lower 16 data lines (D15-0) must be tied together. Bit 3 (BW16) in the DCNTL register (38h) must be set during the initialization so that the SYM53C720 will operate in 16-bit wide mode. The IRQ/ output from the SYM53C720 is not connected in this interface, since polled interrupts are used. If hardware IRQ/ interrupts are to be used, then additional glue logic may be required between the SYM53C720 and the 80386SX.

SCSI Interface

Alternative Two single ended termination is highly recommended, especially when implementing fast SCSI (>5 MB/s). This type of circuit provides better signal quality and a more stable term-power supply. For more information on Alternative Two transition, refer to the SCSI specification.

ABEL Listing

```
module SYM53C720;
title 'Address decoder for 53C720 board'

U12 device ‘P22v10’;

VCC, GND                                                                    pin 24, 12
A23, A22, A21, A20, A19, A18, A17, A16, A15                 pin 2, 3, 4, 5, 6, 7, 8, 9, 10;
A14, A13, A12, A11, A10, A9, A8, A7                      pin 23, 22, 21, 20, 19, 18, 17, 16;
ADS, READYO, CS                                                          pin 11, 15, 14;

X=.X.;
ADDR = [A23, A22, A21, A20, A19, A18, A17, A16, A15, A14, A12, A12, A11, A10, A9, A8, A7];

equations

!CS = (READYO & !ADS & (ADDR == ^hD000)); “E000 ROM CARTRIDGE AREA

test_vectors ([ADDR, ADS, READYO] -> [CS])
[[X,X,X,X,X,X,X,X,X,X,X,X,X,X,X,X,X],1,X] -> [1];
[[X,X,X,X,X,X,X,X,X,X,X,X,X,X,X,X,X],X,0] -> [1];
[^hCfff, 0, 1] -> [1];
[^hD000, 0, 1] -> [0];
[^hD001, 0, 1] -> [1];

end SYM53C720
```

ABEL Listing

```
       module SYM53C720
title'53C720 signals -> 80386SX signals'

u23 device 'P16v8r':

VCC, GND, BCLK                                                          pin 20, 10, 1;
INTELHLDA, SYMMASTER, SYMHOLD, SYMTT0, SYMFETCH, INTELRESET           pin 2, 3, 4, 5, 6, 7;
SYMHLDAI, INTELHOLD, SYMM_IO, SYMRESET                                 pin 19, 18, 17, 16;

ON,OFF                                                                          = 1, 0;
X, Z                                                                          =.X., .Z.;

equations

INTELHOLD = !(!SYMHOLD & !SYMMASTER);
SYMHLDAI = !INTELHLDA;
SYMRESET = !INTELRESET;
SYMM_IO.OE = !SYMMASTER;

truth_table ([SYMFETCH, SYMTT0] -> [SYMM_IO])
"INPUT        OUTPUT
"SYMFETCH SYMTT0
[0,0] -> [1];"Fetch-low=memory, TT0-low=i/o -> memory access
[0,1] -> [1];"Fetch-low=memory, TT0-high=memory -> memory access
[1,0] -> [0];"Fetch-high=i/o, TT0-low=i/o -> i/o access
[1,1] -> [1];"Fetch-high=io, TT0-high=memory -> memory access

test_vectors ([SYMHOLD, SYMMASTER] -> [INTELHOLD])
[ON,OFF] -> [ON];
[OFF, ON] -> [ON];
[ON, ON} -> [ON];
[OFF, OFF] -> [OFF];

test_vectors ([INTELHLDA] -> [SYMHLDAI])
[OFF] -> [ON];
[ON] -> [OFF];

test_vectors ([SYMFETCH, SYMTT0, SYMMASTER] -> [SYMM_IO])
[X,X,1] -> [Z];

test_vectors ([INTELRESET] -> [SYMRESET])
[OFF] -> [ON];
[ON] -> [OFF];

end SYM53C720
```

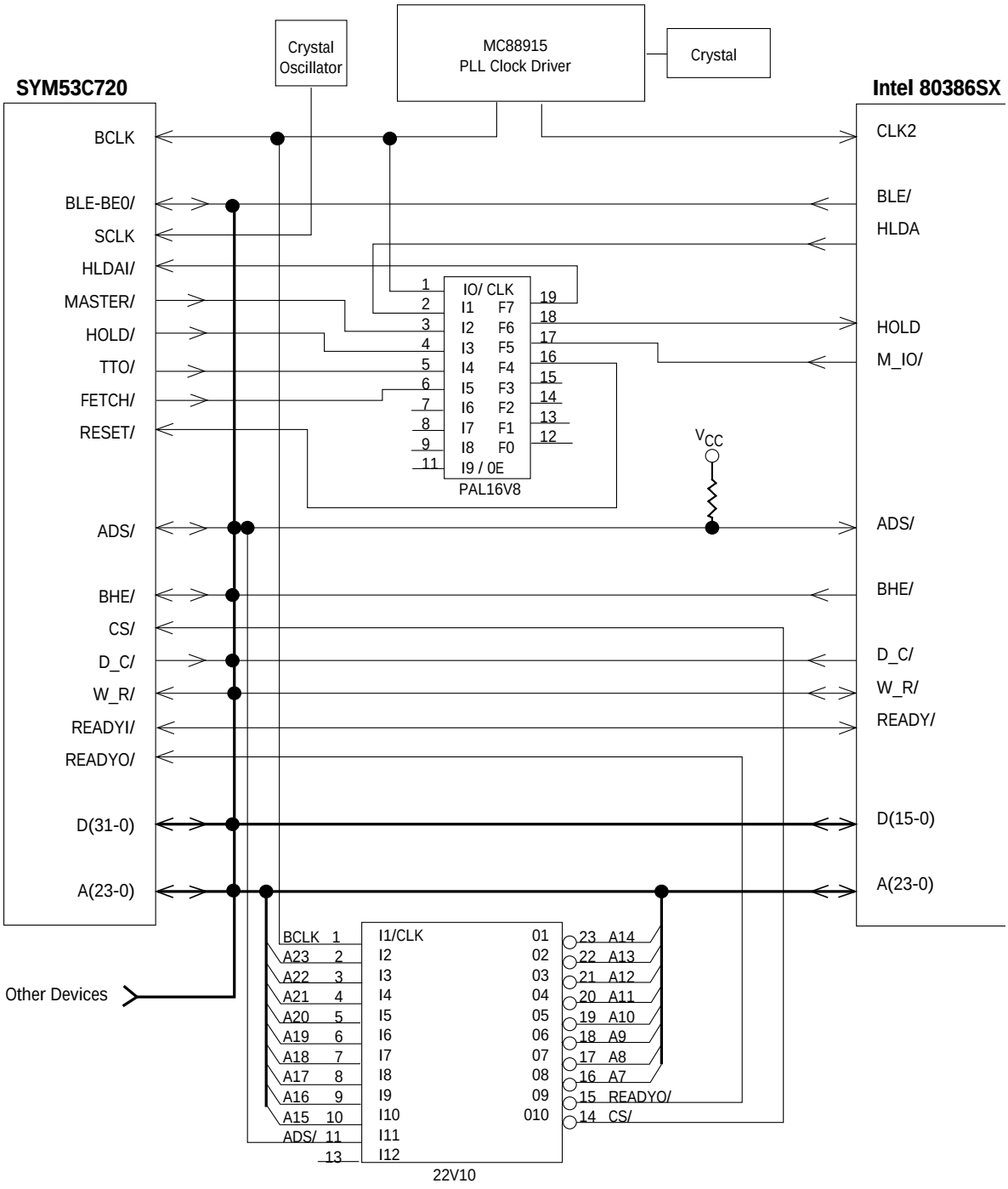

Figure 1. SYM53C720 to 80386SX Interface