System Engineering Notes
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SYM53C710 to SYM53C720 Comparison
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INTRODUCTION

This engineering note compares the SYM53C720 with the SYM53C710. There are four categories of SYM53C720 differences.

A. Host Bus Interface Differences
B. SCRIPTS Instruction Differences
C. SCSI Bus Interface Differences
D. Register Differences

FEATURES

The "Features" section summarizes the high-level differences.

FEATURES	SYM53C710	SYM53C720
1. SCSI Data Transfer Rate		
- Asynchronous	5 Mbytes/sec	10 Mbytes/sec
- Synchronous	10 Mbytes/sec	20 Mbytes/sec
2. DMA Transfer Rate	66 Mbytes/sec	105 Mbytes/sec
3. Host Bus Width	32 bits	16 or 32 bits
4. SCSI Bus Width	8 bits	8 or 16 bits
5. Interrupt On-The-Fly	Not Supported	Supported
6. Bus Modes	4	7
7. SCRIPTS Auto-Start	Not Supported	Supported
8. Programmable Burst Length	1, 2, 4 or 8	2, 4, 8 or 16
9. Shadowed Temp and DSA Registers	Not Supported	Supported
10. Programmable SCSI Timers	Not Supported	3
11. General Purpose I/O Pins	Not Supported	Supported
12. Differential Sense Pin	Not Supported	Supported
13. Preview of Next Address	Not Supported	Supported
14. Carry Bit In ALU	Not Supported	Supported
15. Semaphore Bit	Not Supported	Supported
16. Devices on SCSI Bus	8	16
17. Host Parity Checking	Not Supported	Supported

A. HOST BUS INTERFACE DIFFERENCES

The SYM53C720 host bus interface has been significantly enhanced over that of the SYM53C710. Greater flexibility and functionality has been provided allowing the SYM53C720 to directly interface with a larger number of host busses. The SYM53C720 is still compatible signal for signal with the SYM53C710 host bus interface. The SYM53C720 host bus interface differences are as follows:

Bus Mode Select Pins

Function

The SYM53C720 is capable of interfacing with host busses in a combination of the following modes: Motorola or Intel, Big or Little Endian, 68040_68030 or 80386dx_80386sx. If Intel and one of the 80386 modes is selected, several pins change functions. In particular the R_W/ pin becomes inverted and SIZ0, SIZ1, A0 and A1 become byte enable signals. The SYM53C710 is only capable of interfacing with host busses in a combination of the following modes without external hardware: Big or Little Endian, 68030 or 68040.

Benefit

The ability to interface with seven different host processor busses provides the user with additional flexibility.

Enhanced Cache-Line Burst

Function

Cache-Line burst eliminates the need for a full handshake between the SYM53C720 bus and the memory device when transferring data. The bus master will arbitrate for the bus at the beginning of a 16 byte transfer and it is able to transfer one long word per clock period. The SYM53C720 is able to start another cache-line burst without getting off the bus if it has another 8 long words stored in its FIFO. Under optimal conditions the SYM53C720 will have 16 long words in its FIFO and it is therefore able to do four back-to-back cache transfers. A cache line burst is always 4 long words in length. The SYM53C710 was only capable of doing one cache-line burst before it had to get off the bus.

Benefit

Cache-Line Burst mode allows up to 105 Mbytes/sec DMA burst bandwidth for extremely high data transfer rates or streaming modes. The SYM53C710 is only capable of doing 66 Mbytes/sec DMA transfers.

Sense Pin for SCRIPTS Auto-Start

Function

When the SCRIPTS auto-start sense pin is tied to ground the DMA SCRIPTS Pointer Register (DSP) points to an address of all zeros and the SCRIPTS processor will start fetching instructions from that location. If the sense pin is tied high, the DSP register will have to be written with the starting address of the first SCRIPTS instruction.

Benefit

The auto-start feature enables the SYM53C720 to start the SCRIPTS program automatically after reset is deasserted. SCRIPTS instructions will be fetched and executed until an interrupt condition occurs.

General Purpose Input and Output Pins

Function

The SYM53C720 has four inputs and one output pin. These pins are user defined.

Benefit

The input pins may be used to read the SYM53C720 chip ID or other configuration information. The output pin may be used to enable on-board ROM, RAM or LEDs.

Memory Access Control Pin

Function

This signal indicates if the next access will be to local memory (on-board memory) or far memory (system memory).

Benefit

The ability to choose between near and far memory provides system design flexibility, with faster access to data in local memory.

Test In and Test Out Pins

Function

These pins connect all inputs and outputs (excluding SCSI control signals and data lines) to an AND tree test scheme.

Benefit

This function allows manufacturers to verify chip connectivity to the board, and to determine exactly which pins are not properly attached.

B. SCRIPTS INTRODUCTION DIFFERENCES

Five SCRIPTS instructions have been added to the SYM53C720. The SYM53C720 utilizes all of the SCRIPTS instructions available for the SYM53C710, therefore, SCRIPTS programs developed for the SYM53C710 will be upward compatible. For a more detailed description of the SCRIPTS language, reference the SYM53C720 Programmer's Guide. Following is a list and description of the five instructions.

CHMOV Instruction

Function

The CHMOV instruction transfers data to and from memory locations. Data may come from any data location, so scatter/gather operations are transparent to the chip and the external processor.

Benefit

When the SYM53C720 executes several CHMOV instructions and one ends on an odd byte boundary, the SYM53C720 temporarily stores the residual byte. The SYM53C720 takes the first byte from the subsequent CHMOV or MOVE instruction and lines it up with the residual byte in order to complete a wide transfer and maintain a continuous data flow of the SCSI bus.

INTFLY Instruction

Function

The INTFLY instruction (DBC, bit 20) will assert the Interrupt on the Fly bit (ISTAT, bit 2) once the SCRIPTS instruction is executed. SCRIPTS programs will not halt when the interrupt occurs. The interrupt must be serviced by reading the Interrupt Status Register only.

Benefit

The INTFLY instruction is used to notify a service routine, running on the main processor, while the SCRIPTS processor is still executing a SCRIPTS program.

Transfer Control Instruction on Carry

Function

Jump, Call, Return or Interrupt may be executed depending on the resulting carry bit (DBC, bit 21) after an add operation. When executing a transfer control instruction true/false comparisons are legal whereas compare functions are illegal. As an example, INT address, IF carry and INT address, IF NOT carry would be legal.

Benefit

The transfer control on carry feature adds additional flexibility to the user by allowing additions to cross byte boundaries.

Read/Write Instruction WITH Carry Enabled

Function

When carry is enabled (DCMD, bit 0) any read/write opcode utilizing the add operation will also add in the current carry contents. MOVE SCRATCH1 + 1 To SCRATCH1 WITH Carry, is an example.

Benefit

Enabling the carry bit allows the SYM53C720 to perform add operations greater than one byte, since carry values from previous byte adds may be used in successive adds.

I/O Instruction SET or CLEAR Carry

Function

The Carry bit may be SET or CLEARed using a SCRIPTS Instruction (DBC, bit 10)

Benefit

This feature permits the user to assert or deassert the carry bit prior to an addition or subtraction operation.

C. SCSI BUS INTERFACE DIFFERENCES

The primary difference between the SYM53C710 and the SYM53C720 is the implementation of Wide SCSI. The SYM53C720 differences are as follows:

Wide SCSI

Function

The SYM53C720 has a 16-bit data transfer capability. There is a single request/acknowledge per transfer and the SCSI bus pinout is optimized for P or A cable connection.

Benefit

Wide SCSI provides a significant increase in system performance especially in systems requiring a large amount of data transfer between host and peripheral devices. The SYM53C720, as a result of wide SCSI, transfers data over the SCSI bus at up to 20 Mbytes/sec whereas the SYM53C710 transfers data at up to 10 Mbytes/sec. This applies only when the SCSI bus is operating in synchronous and differential modes.

Differential Sense Pin

Function

The SYM53C720 uses the Differential Sense pin to determine if a connected SCSI device is operating in differential or single ended mode. If the external device is operating in differential mode while the SYM53C720 is in single ended mode, the chip will cease to drive external outputs on the SCSI bus.

Benefit

The sense pin protects the external differential pair transceivers and the single ended device from damage.

SCSI Clock

Function

The SYM53C720 has a separate SCSI clock which operates at up to 75 MHz. The SYM53C710 operates the SCSI clock at up to 50 MHz.

Benefit

Separate SCSI and bus clocks allow the host interface to operate at a lower speed while a higher speed clock controlling the SCSI bus guarantees fast SCSI timings of 20 Mbytes/sec. A clock speed of minimum 40 MHz is required for fast SCSI.

Initiator/Target Auto-Switch Disabled

Function

The auto-switch function is disabled in the SYM53C720.

Benefit

This forces the user to manually set target or initiator mode in a SCRIPTS program and removes any ambiguity as to the current mode of the SYM53C720.

SCSI Timers

Function

The SYM53C720 provides programmable select/reselect, handshake to handshake, and general purpose timers. The time-out period is programmable from 100 µsec to greater than 1.6 seconds. A maskable interrupt is available for each of the timers.

Benefit

The timers allows the user to tailor SCRIPTS instructions to their specific timeout needs.

Separation of Selection and Reselection Control

Function

The SYM53C720 can be enabled to respond as a target, initiator or both. There are status and interrupt bits indicating that the SYM53C720 has responded to selection or reselection.

Benefit

The SYM53C720 will know if it is required to respond as an initiator or a target. If the user has disabled selection and another SCSI device actually tries to select the SYM53C720, it may notify the main processor that this has occurred.

D. REGISTER DIFFERENCES

The following figures summarize the differences between the SYM53C710 and the SYM53C720 register sets. The register/bit additions and the resulting benefits to the user are described below. For a more detailed explanation of each of the registers in the SYM53C720, reference the SYM53C720 Data Manual.

New Registers/Bits

Registers/Bits	SYM53C710	SYM53C720
Start SCSI Transfer bit	Not Supported	SCNTL1, bit 0
Immediate Arbitration bit	Not Supported	SCNTL1, bit 1
SCSI Control Register Two – 02h	Not Supported	SCNTL2
Wide SCSI Receive bit	Not Supported	SCNTL2, bit 0
Wide SCSI Send bit	Not Supported	SCNTL2, bit 3
Chained Mode bit	Not Supported	SCNTL2, bit 6
SCSI Disconnect Unexpected bit	Not Supported	SCNTL2, bit 7
SCSI Control Register Three – 03h	Not Supported	SCNTL3
Enable Wide SCSI bit	Not Supported	SCNTL3, bit 3
Enable Response to Selection bit	Not Supported	SCID, bit 5
Enable Response to Reselection bit	Not Supported	SCID, bit 6
General Purpose Register – 07h	Not Supported	GPREG
General Purpose Inputs/Outputs	Not Supported	GPREG, bits 4-0
SCSI Selector ID Register – 0Ah	Not Supported	SSID
Encoded Destination SCSI ID Bits	Not Supported	SSID, bits 3-0
SCSI Selector ID Valid bit	Not Supported	SSID, bit 7
SCSI Parity SD 15-8 Bit	Not Supported	SSTAT2, bit 0
Last Disconnect bit	Not Supported	SSTAT2, bit 1
Latched SCSI Parity SD 15-8-Bit	Not Supported	SSTAT2, bit 3
SODL Most Significant Byte Full	Not Supported	SSTAT2, bit 5
SODR Most Significant Byte Full	Not Supported	SSTAT2, bit 6
SIDL Most Significant Byte Full	Not Supported	SSTAT2, bit 7
Interrupt On The Fly bit	Not Supported	ISTAT, bit 2
Semaphore bit	Not Supported	ISTAT, bit 4
Cache 386 Enable bit	Not Supported	CTEST0, bit 0
Generate Receive Parity for Pass Through	Not Supported	CTEST0, bit 4
Host Parity Check Enable bit	Not Supported	CTEST4, bit 3
Shadow Register Test Mode bit	Not Supported	CTEST4, bit 4
SCSI Data Bus High Impedance Mode	Not Supported	CTEST4, bit 5
Enable Host Parity Error Interrupt	Not Supported	DIEN, bit 6
Host Bus Width 16 bits	Not Supported	DCNTL, bit 3
Bus Mode bit	Not Supported	DCNTL, bit 6
Size Throttle Enable bit	Not Supported	DCNTL, bit 7
SCSI Interrupt Enable Register One – 41h	Not Supported	SIEN1
Handshake Timer Expired	Not Supported	SIEN1, bit 0
General Purpose Timer Expired	Not Supported	SIEN1, bit 1
SCSI Interrupt Status Register Zero – 42h	Not Supported	SIST0
SCSI Interrupt Status Register One – 43h	Not Supported	SIST1
SCSI Wide Register – 45h	Not Supported	SWIDE
Memory Access Control Register – 46h	Not Supported	MACNTL
General Purpose Control Register – 47h	Not Supported	GPCNTL

NOTE: The addresses refer to Little Endian byte orientation.

New Registers/Bits (continued)

Registers/Bits	SYM53C710	SYM53C720
SCSI Time Register Zero – 48h	Not Supported	STIME0
Programmable Select/Reselect Timer	Not Supported	STIME0, bits 3-0
Programmable Handshake Timer	Not Supported	STIME0, bits 7-4
SCSI Time Register One – 49h	Not Supported	STIME1
Response ID Zero Register – 4Ah	Not Supported	RESPID0
Response ID One Register – 4B	Not Supported	RESPID1
SCSI Test Register Zero – 4Ch	Not Supported	STEST0
SCSI Synchronous Offset Max. bit	Not Supported	STEST0, bit 0
SCSI Synchronous Offset Min. bit	Not Supported	STEST0, bit 1
Arbitration Priority Test bit	Not Supported	STEST0, bit 2
Selection Response Logic bit	Not Supported	STEST0, bit 3
SCSI Test Register One – 4Dh	Not Supported	STEST1
SCSI Test Register Two – 4Eh	Not Supported	STEST2
Extended REQ/ACK Filtering bit	Not Supported	STEST2, bit 1
Always Wide SCSI bit	Not Supported	STEST2, bit 2
SCSI Control Enable bit	Not Supported	STEST2, bit 7
SCSI Test Register Three -- 4Fh	Not Supported	STEST3
SCSI FIFO Test Write bit	Not Supported	STEST3, bit 0
Clear SCSI FIFO bit	Not Supported	STEST3, bit 1
Timer Test Mode bit	Not Supported	STEST3, bit 2
16-bit System	Not Supported	STEST3, bit 3
Disable Single Initiator Response	Not Supported	STEST3, bit 4
Halt SCSI Clock bit	Not Supported	STEST3, bit 5
SCSI FIFO Test Read bit	Not Supported	STEST3, bit 6
TolerANT Enable	CTEST0, bit 4	STEST3, bit 7
SCSI Input Data Latch bits 15-8	Not Supported	SIDL
SCSI Output Data Latch bits 15-8	Not Supported	SODL
SCSI Bus Data Lines bits 15-8	Not Supported	SBDL
General Purpose Scratch Pad Register 1 – 5C-5Fh	Not Supported	SCRATCH1

Note: The addresses refer to Little Endian byte orientation.

Deleted Registers/Bits

Registers/Bits	SYM53C710	SYM53C720
Start SCSI Receive Operation bit	SCNTL1, bit 0	Not Supported
Start SCSI Send Operation bit	SCNTL1, bit 1	Not Supported
Enable Selection and Reselection	SCNTL1, bit 5	Not Supported
SCSI Destination ID bits 7-4	SDID bit 7-4	Not Supported
SCSI Chip ID bits 7-4	SCID bit 7-4	Not Supported
SCSI Offset Compare bit	CTEST2, bit 5	Not Supported
SCSI FIFO Write Enable bit	CTEST4, bit 3	Not Supported
DACK/ bit	CTEST5, bit 0	Not Supported
DREQ/ bit	CTEST5, bit 1	Not Supported
EOP bit	CTEST5, bit 2	Not Supported
Chip Test Register Seven	CTEST7	Not Supported

Note: The addresses refer to Little Endian byte orientation.

Moved Registers/Bits

Registers/Bits	SYM53C710	SYM53C720
SCSI Destination ID Register (SDID)	Address 02h	Address 06h
SCSI Interrupt Enable Register (SIEN)	Address 03h	Address 40h
SCSI Synchronous Transfer Period	SXFER, bits 6-4	SXFER, bit 7-5
Disable Halt on Parity Error or ATN bit	SXFER, bit 7	SCTRL1, bit 5
SCSI Output Data Latch Register (SODL)	Address 06h	Address 54-55h
SCSI Output Control Latch Register (SOCL)	Address 07h	Address 09h
SCSI Input Data Latch Register (SIDL)	Address 09h	Address 50-51h
SCSI Bus Data Line Register (SBDL)	Address 0Ah	Address 58-59h
Synchronous SCSI Clock Frequency	SBCL, bits 1-0	SCNTL3, bit 6-4
SCSI RST/ Received bit	SSTAT0, bit 1	SIST0, bit 1
Unexpected Disconnect bit	SSTAT0, bit 2	SIST0, bit 2
SCSI Gross Error bit	SSTAT0, bit 3	SIST0, bit 3
Function Complete bit	SSTAT0, bit 6	SIST0, bit 6
Phase Mismatch or ATN/ Active bit	SSTAT0, bit 7	SIST0, bit 7
SCSI Status Register One	SSTAT1	SSTAT0
SCSI Status Register Two	SSTAT2	SSTAT1
Chip Test Register Zero (CTEST0)	Address 14h	Address 18h
Data Transfer Direction bit	CTEST0, bit 0	CTEST2, bit 7
Chip Test Register One (CTEST1)	Address 15h	Address 19h
Chip Test Register Two (CTEST2)	Address 16h	Address 1Ah
SCSI FIFO Parity (bits 7-0) bit	CTEST2, bit 4	STEST1, bit 0
Chip Test Register Three (CTEST3)	Address 17h	Address 1Bh
Chip Test Register Four (CTEST4)	Address 18h	Address 21h
SCSI Loopback Enable bit	CTEST4, bit 4	STEST2, bit 4
SCSI High Impedance Mode bit	CTEST4, bit 5	STEST2, bit 3
Chip Test Register Five (CTEST5)	Address 19h	Address 22h
Reset SCSI Offset bit	CTEST5, bit 5	STEST2, bit 6
Chip Test Register Six (CTEST6)	Address 1Ah	Address 23h
Transfer Type bit	CTEST7, bit 1	CTEST0, bit 1
Even Parity - Host Bus bit	CTEST7, bit 2	CTEST0, bit 2
DMA FIFO Parity bit	CTEST7, bit 3	CTEST0, bit 3
Snoop Control bits 1-0	CTEST7, bit 6-5	CTEST0, bits 6-5
Cache Burst Disable bit	CTEST7, bit 7	CTEST0, bit 7
Chip Test Register Eight	CTEST8	CTEST3
Interrupt Status Register (ISTAT)	Address 21h	Address 14h
Longitudinal Parity Register	LCRC 23h	SLPAR 44h
Enable Low Level SCSI Mode	DCNTL, bit 3	STEST2, bit 0
Clock Frequency bits	DCNTL, bit 7-6	SCNTL 3, 2-0

Note: The addresses refer to Little Endian byte orientation.

Start SCSI Transfer Bit

Function

The start SCSI transfer bit (SCNTL1, bit 0) has been added to initiate SCSI transfers. The SYM53C720 automatically sets the bit when a transfer operation is executed. It can be determined if the transfer is send or receive depending on the value written to the I/O bit in the SCSI Output Control Latch Register. The SYM53C710 possessed two bits to indicate that the chip was starting a send or receive operation.

Benefit

This bit is used for test purposes only and it is automatically set in low level mode and during SCRIPTS execution.

Immediate Arbitration Bit

Function

Asserting the immediate arbitration bit (SCNTL1, bit 1) will prompt the SYM53C720 to arbitrate immediately after a disconnect has occurred.

Benefit

The immediate arbitration bit permits the SYM53C720 to participate in the next arbitration after a disconnect. This bit is useful for multi-threaded applications. The SYM53C710 was not capable of joining and winning arbitration immediately after a disconnect.

Wide SCSI Receive Bit

Function

The wide SCSI receive bit (SCNTL2, bit 0) is asserted when the SYM53C720 detects a possible partial transfer at the end of a block move instruction. This residual byte is stored in the SCSI Wide Residue Data Register until the subsequent transfer. At this point the SYM53C720 can determine if the byte was “residual” data, valid data for a subsequent transfer, or overrun data. This byte will be combined with another byte during the subsequent receive operation if the data is valid.

Benefit

This bit allows the data within multiple block move instructions to be chained together. If a move instruction ends on a odd byte boundary the next move instruction will provide the additional byte so that a word transfer will occur.

Wide SCSI Send Bit

Function

The wide SCSI send bit (SCNTL2, bit 3) is asserted at the start of a wide SCSI send operation. If the transfer ends on an odd byte boundary, the bit will still be asserted at the end of the transfer. This indicates that the low order byte of the SCSI Output Data Latch Register contains the last byte from the current send operation. The low order byte will be combined with the high order byte of the subsequent send operation.

Benefit

This bit allows the data within multiple block move instructions to be chained together. If a move instruction ends on a odd byte boundary, the next move instruction will provide the high order byte so that a word transfer will occur.

Chained Mode Bit

Function

The chained mode bit (SCNTL2, bit 6) allows for chained block move instructions. The SCRIPTS processor automatically sets the bit when a chained block move instruction is executed. The processor resets the bit when a regular block move SCRIPTS instruction is executed.

Benefit

When this bit is set and a data transfer ends on an odd byte boundary the SYM53C720 will store the last byte in the SCSI Wide Residue Data Register during a receive operation or in the SCSI Output Data Latch Register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wise transfer can be completed.

SCSI Disconnect Unexpected Bit

Function

The SCSI disconnect unexpected bit (SCNTL2, bit 7) should be asserted if the SYM53C720 is not expecting the SCSI bus to enter the bus free phase. The SYM53C720 automatically sets this bit when it is selected, reselected, performs a selection, or a reselection. The bit only has meaning in initiator mode.

Benefit

The SYM53C720 uses this bit to determine if the disconnect was expected. If the chip enters a bus free phase and the bit is set, an unexpected disconnect error will be generated in the SCSI Interrupt Status Register Zero.

Enable Wide SCSI Bit

Function

The wide SCSI bit (SCNTL3, bit 3) enables 16-bit data transfers over the SCSI bus. The bit is cleared for 8-bit only data transfers.

Benefit

Wide SCSI operation allows the SYM53C720 to double its data transfer rate across the SCSI bus.

Selection and Reselection Control Bits

Function

The selection enable bit (SCID, bit 5) should be asserted when the SYM53C720 is required to respond as a target and the reselection enable bit (SCID, bit 6) should be asserted when the SY53C720 is required to respond as an initiator. There are also status and interrupt bits indicating whether or not the SYM53C720 has been selected or reselected. The SYM53C710 only contains one bit indicating that the chip had been selected/reselected.

Benefit

The selection or reselection enable bit allows the SYM53C720 to respond as either an initiator or a target device. For example, if only selection is enabled, the SYM53C720 cannot be reselected as an initiator. The status and interrupt bits can be polled so the appropriate target or initiator SCRIPTS can be executed. These bits also make it possible to determine whether the SYM53C720 has been selected or reselected.

General Purpose Input/Output Bits

Function

The general purpose bits (GPREG, bits 4-0) allow the SYM53C720 to detect the input signals of a connected device, or to enable attached ROM, RAM, or LEDs on a SYM53C720 board. The pins all have internal pull-ups.

Benefit

The general purpose input feature can be used to sense the SYM53C720 chip ID or board configuration at power up. A register to Register Move instruction may be used to move the sensed value into the appropriate register.

SCSI Selector ID Valid Bit and Encoded Destination SCSI ID Bits

Function

SCSI selector valid ID bit (SSID, bit 7) will automatically be set when two SCSI IDs are detected on the bus during a bus-initiated selection or reselection. The encoded destination ID bits (SSID, bits 3-0) contain the ID of the initiator, selecting the SYM53C720, or the ID of the target, re-selecting the SYM53C720. The destination ID is valid when the selector ID is set.

Benefit

This bit enhances the development of multi-threaded I/O SCRIPTS. The SYM53C720 will, with greater ease, be able to support disconnects with the knowledge of the selector or re-selector's ID.

SCSI Data Parity One Signal

Function

The SCSI data parity one signal (SSTAT2, bit 0) represents the parity on the high order byte lane. The parity signal is unlatched and may be changing at any time.

Benefit

The SCSI Parity signal is used to detect parity errors on the upper byte lane during wide data transfer.

Last Disconnect Bit

Function

The last disconnect bit (SSTAT2, bit 1) is used in conjunction with the connected bit in the SCSI Control Register One to determine if a disconnect and then a selection or reselection of the SYM53C720 has occurred. If the connected bit is asserted and the last disconnect bit is asserted, a disconnect has occurred. The bit is also asserted at chip reset indicating a disconnect state.

Benefit

The last disconnect bit, in conjunction with the connected bit, notifies the SYM53C720 that a disconnect has transpired and that the SYM53C720 is again connected to a SCSI device. Every time the last disconnect bit is set after a CHMOV instruction has been executed, a disconnect has occurred since the prior CHMOV instruction.

Latched SCSI Data Parity One Signal

Function

The latched SCSI data parity one signal (SSTAT2, bit 3) represents the odd parity of the high order byte in a 16-bit data transfer. The data is latched in the most significant byte of the SCSI Input Data Latch Register.

Benefit

The SCSI parity signal is used to detect parity errors on the upper byte lane in 16-bit data transfers.

SCSI Output Data Latch Most Significant Byte Full

Function

The SCSI output data latch most significant byte full bit (SSTAT2, bit 5) is asserted when the high order byte is written to the SCSI Output Data Latch Register (SODL) during a synchronous or an asynchronous SCSI send operation. The bit is deasserted when the byte is transferred from the SODL register to the SCSI bus during an asynchronous send, or to the internal SCSI Output Data Register during a synchronous send.

Benefit

This bit is sued to determine if the high order byte remains in the SCSI Output Data Latch Register when the chip halts a data transfer operation. The allows for restoration of data pointers after an interrupt.

SCSI Output Data Register Most Significant Byte Full

Function

The SCSI output data register most significant byte full bit (SSTAT2, bit 6) is asserted when the high order byte is written to the SCSI Output Data Register during a synchronous SCSI send operation. The bit is deasserted when the byte is transferred to the SCSI bus during a synchronous send operation.

Benefit

This bit is used to determine if the high order byte remains in the SCSI Output Data Register when the chip halts a data transfer operation. This allows for restoration of data pointers after an interrupt.

SCSI Input Data Latch Most Significant Byte Full

Function

The SCSI input data latch register most significant byte full bit (SSTAT2, bit 7) is asserted when the high order byte is written to the SCSI Input Data Latch Register (SIDL) during an asynchronous SCSI receive operation. The bit is deasserted when the byte is transferred to the SIDL register to the DMA FIFO.

Benefit

This bit is used to determine if their is a higher order byte in the SCSI Input Data Latch Register. This allows the SCRIPTS processor to finish transferring data into memory after an interrupt.

Interrupt on the Fly Bit

Function

The interrupt on the fly bit (ISTAT, bit 2) can be asserted by an interrupt instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. The interrupt must be serviced by reading the Interrupt Status Register only.

Benefit

This bit can be used to notify a service routine, running on the main processor, while the SCRIPT processor is still executing a SCRIPTS program.

Semaphore Bit

Function

The semaphore bit (ISTAT, bit 4) can be set by the SCRIPTS processor using a SCRIPTS register write. The bit may also be set by an external processor while the SYM53C720 is executing a SCRIPT.

Benefit

This bit enables the SYM53C720 to notify the external processor of a predefined condition while SCRIPTS are running. The processor may also notify the SYM53C720 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

Generate Receive Parity for Pass Through Bit

Function

When this bit is set and the SYM53C720 is in parity pass through mode, parity received on the SCSI bus will not pass through the DMA FIFO. Parity will be generated as data enters the DMA FIFO, eliminating the possibility of bad SCSI parity passing through the host bus.

Benefit

This bit isolates SCSI parity errors to the SYM53C720 instead of passing on bytes with bad parity to the system.

Host Parity Check Enable bit

Function

Asserting the host parity check enable bit (CTEST4, bit 3) enables parity checking during slave write and DMA read execution. The system powers up with this bit disabled so that the SYM53C720 will function properly with systems that do not support parity.

Benefit

This bit may be enabled by the user for additional flexibility.

Shadow Register Test Mode

Function

Asserting the shadow register test mode bit (CTEST4, bit 4) allows the user to read the Shadowed Temporary Stack (TEMP) and Data Structure Address Registers (DSA).

Benefit

The assertion of this bit allows the user to retrieve data previously stored in these registers. These registers are “shadowed” because both are written over during a Memory to Memory Move operation. The TEMP and DSA registers contain the base address, used for all table indirect calculations, and the instruction address pointer respectively.

SCSI Data Bus High Impedance Mode

Function

Asserting the SCSI data bus high impedance mode bit (CTEST4, bit 5) places the SCSI data bus and parity lines in a high-impedance state.

Benefit

This bit is used for functional or burn-in testing.

Enable Host Parity Error Interrupt

Function

Asserting the host parity error interrupt bit (DIEN, bit 6) causes the SYM53C720 to generate a hardware interrupt when a parity error is detected at the host interface. If the bit is cleared the external IRQ/ signal will not be asserted.

Benefit

This bit is used to notify the main processor that a parity error has occurred at the host interface.

Host Bus Width Equal to 16-Bits

Function

When the host bus width equal to 16-bit (DCNTL, bit 3) is set the SYM53C720 host interface will convert to a 16-bit wide bus. (Note: data lines 31-16 must be tied to data lines 15-0). The default mode is 32 bits at the host interface.

Benefit

This bit allows the SYM53C720 to operate with a 16-bit host bus.

Bus Mode Bit

Function

The assertion of the bus mode bit (DCNTL, bit 6) gives the function code pins new meaning. The bit should only be asserted when the SYM53C720 is in 80386sx or 80386dx mode or is not used in a native 68030 or 68040 environment. FC0 remains unaffected and provides a data control signal. FC1 becomes reserved and FC2 becomes an input to allow preview of next addresses.

Benefit

The assertion of this bit enables the SYM53C720 to interface, with greater ease, to the EISA bus.

Size Throttle Enable Bit

Function

This bit causes the SYM53C720 to relinquish bus ownership every time the transfer size changes.

Benefit

This allows the SYM53C720 to interface to host buses that do not allow size changes within a bus ownership.

Handshake-to-Handshake Timer Expired Interrupt Enable

Function

Assertion of the handshake-to-handshake timer expired interrupt enable bit (SIEN1, bit 0) prompts the SYM53C720 to generate a hardware interrupt when the handshake-to-handshake timer has expired. The time measured is the SCSI REQuest to REQuest or ACKnowledge to ACKnowledge period. The time-out period is programmed in the SCSI Timer Register ZERO, bits 7-4. Possible timeout values range from 100 microseconds to greater than 1.6 seconds. If the bit is cleared the external IRQ/signal will not be asserted.

Benefit

The bit is used to notify the main processor that the timeout period has expired.

General Purpose Timer Expired Interrupt Enable

Function

Assertion of the general purpose timer expired interrupt enable bit (SIEN1, bit 1) prompts the SYM53C720 to generate a hardware interrupt when the general purpose timer has expired. The timeout period is programmed in the SCSI Timer Register One, bits 3-0. Possible timeout values range from 100 microseconds to greater than 1.6 seconds. If the bit is cleared the external IRQ/ signal will not be asserted.

Benefit

The bit is used to notify the main processor that the timeout period has expired.

SCSI Interrupt Status Zero Register

Function

The SCSI interrupt status zero register returns the status of the various interrupt conditions that can occur in the SCSI Interrupt Enable Register Zero.

Benefit

Each bit value asserted indicates that a corresponding interrupt condition has occurred. The bits have to be polled since the external IRQ/ signal will not be asserted.

SCSI Interrupt Status Register One

Function

The SCSI interrupt status one register returns the status of the various interrupt conditions that can occur in the SCSI Interrupt Enable Register One.

Benefit

Each bit value asserted indicates that a corresponding interrupt condition has occurred. The bits have to be polled since the external IRQ/ signal will not be asserted.

SCSI Wide Residue Data Register

Function

The SCSI wide residue data register contains a residual byte, the first byte of a subsequent transfer, or an overrun data byte.

Benefit

If an Ignore Wide Residue message is not received the wide residue data should become part of the next data transfer.

Response ID Zero and Response ID One Registers

Function

These registers contain the selection or reselection IDs that the chip responds to on the SCSI bus. Each bit represents one possible ID.

Benefit

These registers allow the SYM53C720 to respond to more than one ID. However, the chip can arbitrate with only one ID value in the SCID register.

Programmable Select/Reselect Timeout Timer

Function

A select/reselect timer (STIME0, bits 3-0) will, if activated, interrupt the SYM53C720 if the chip has not been selected or reselected within a user defined time period. The timer is programmable from 100 microseconds to greater than 1.6 seconds. The SYM53C710 used the Selection/Reselection Timer and the timeout period was fixed to be 250 msec.

Benefit

The select/reselect timer within the SYM53C720 is provided so that the system does not have to furnish it in software. The select/reselect timeout period required by the SCSI specification is 250 msec.

Programmable Handshake Timeout Timer

Function

A handshake timer (STIME0, bits 7-4) will, if activated, interrupt the SYM53C720 if the chip has not monitored a transfer within a predefined time period. The time measured is the SCSI REQuest to REQuest or ACKnowledge to ACKnowledge period. The timer is programmable from 100 microseconds to greater than 1.6 seconds. The SYM53C710 used the Section/Reselection Timer and the timeout period was fixed to be 250 msec.

Benefit

The handshake timer is provided so that the system does not have to furnish it. The interrupt will inform the SYM53C720 that the connected SCSI device is not responding.

Programmable General Purpose Timer

Function

A general purpose timer (STIME1, bits 3-0) will, if activated, interrupt the SYM53C720 once a predefined time period has expired. The timer is programmable from 100 microseconds to 1.6 seconds.

Benefit

The general purpose timer may be used to limit the time the SYM53C720 spends on or off the bus. Once the interrupt occurs, after the predefined time period has elapsed, a SCRIPT Disconnect instruction may be executed to free the bus or a Select instruction may be issued to get back on the bus.

SCSI Synchronous Offset Maximum Bit

Function

The SCSI synchronous offset maximum bit (STEST0, bit 0) indicates that the current synchronous SCSI REQ/ACK offset is the maximum specific by bits 3-0 in the SCSI Transfer register. This bit is not latched and may change at any time. The SYM53C710 incorporated this function in the CTEST2 register, bit 5.

Benefit

This bit is used in low level synchronous SCSI operations. When this bit is set the SYM53C720, as a target, is waiting for the initiator to ACKnowledge the data transfers. If the SYM53C720 is an initiator then the target has sent the offset number of REQuests.

SCSI Synchronous Offset Zero Bit

Function

The SCSI synchronous offset zero bit (STEST0, bit 1) indicates that the current synchronous SCSI REQ/ACK offset is zero. This bit is not latched and may change at any time. The SYM53C710 incorporated this function in the CTEST2 register, bit 5.

Benefit

This bit is used in low level synchronous SCSI operations. When this bit is set the SYM53C720, as an initiator, is waiting for the target to REQuest data transfers. If the SYM53C720 is a target then the initiator has sent the offset number of ACKnowledges.

Arbitration Priority Encoder Test Bit

Function

The arbitration priority encoder test bit (STEST0, bit 2) will always be asserted when the SYM53C720 exhibits the highest priority ID asserted on the SCSI bus during arbitration.

Benefit

This bit is primarily used for chip level testing but it may be used during low level mode to determine if the SYM53C720 has won arbitration.

Selection Response Logic Bit

Function

The selection response logic bit (STEST0, bit 3) is asserted when the SYM53C720 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns.

Benefit

This bit is used for functional test and fault purposes.

Extended REQ/ACK Filtering Bit

Function

When the extended REQ/ACK filtering bit (STEST2, bit 1) is asserted, additional filtering on the deasserting edge of the REQ/ and ACK/ signals will be provided. The filter should not be used during fast SCSI transfers (greater than 5 Mbytes/sec).

Benefit

The assertion of this bit will filter out glitches which may be interpreted by the SYM53C720 as assertions of the REQ/ and ACK/ signals.

Always Wide SCSI Bit

Function

When the always wide SCSI bit (STEST2, bit 2) is asserted, all SCSI information transfers are executed in 16-bit mode. In other words, all the phases supported by the SCRIPTS language (message, data, instruction and status) are performed in 16-bit mode.

Benefit

This bit should normally be deasserted since 16-bit wide message, instruction and status phases are not supported by the SCSI specifications. This bit is not guaranteed to function properly with future SCSI wide specifications.

SCSI Control Enable Bit

Function

When the SCSI control enable bit (STEST2, bit 7) is asserted, all the SCSI control and data lines are driven regardless of whether the SYM53C720 is in target or initiator mode.

Benefit

This bit is primarily used for burn-in testing. This bit should not be set during normal operations, since contention on the SCSI bus may otherwise occur.

SCSI FIFO Test Read and Write Bus

Function

These bits place the SCSI core into a test mode in which the SCSI FIFO can be easily written and read.

Benefit

These bits allow additional testing and system diagnostics.

SCSI FIFO Test Mode Bit

Function

Asserting the SCSI FIFO test mode bit (STEST3, bit 0) places the SYM53C720 in a test mode in which the FIFO can easily be read and written.

Benefit

This bit is asserted in order to test the functionality of the FIFO.

Clear SCSI FIFO Bit

Function

Asserting the clear SCSI FIFO bit (STEST3, bit 1) allows the user to clear the flags indicating that the FIFO is full.

Benefit

This bit allows the user to clear the FIFO.

Timer Test Mode Bit

Function

Asserting the timer test mode bit (STEST3, bit 2) allows the user to test the SYM53C720 timers. Setting the bit starts the selection timeout, general purpose, and handshake to handshake timers.

Benefit

This bit is used to facilitate functional testing and increase fault coverage.

16-Bit System

Function

Assertion of the 16-bit system bit (STEST3, bit 3) allows the SYM53C720 to consider 16-bit selection attempts. If parity checking is enabled parity will be checked on the high and low order byte lanes.

Benefit

Wide selection attempts are considered whereas 8-Bit only selection attempts may be ignored due to bad parity since the high order byte lane is not driven.

Disable Single Initiator Response Bit

Function

When the disable single initiator response bit (STEST3, bit 4) is asserted, the SYM53C720 will ignore all bus- initiated selection attempts which employ the single initiator option of SCSI-1.

Benefit

This bit may be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response by the SYM53C720.

Halt SCSI Clock Bit

Function

When the halt SCSI clock bit (STEST3, bit 5) is asserted, the SCSI clock will stop in a glitchless manner. Deasserting the bit will start the clock without glitches.

Benefit

This bit may be used for test purposes or to lower I_{DD} during a power down mode. (SCSI registers must be re-initialized upon power-up).

SCSI Input Data Latch Bits

Function

Bits 15 through 8 in the SCSI Input Data Latch Register were added to accommodate the SYM53C720's wide SCSI data transfer capability. This register is utilized during asynchronous data receive.

Benefit

The addition of these bits allows the SYM53C720 capable of concurrently receiving 16 bits of data.

SCSI Output Data Latch Bits

Function

Bits 15 through 8 in the SCSI Output Data Latch Register were added to accommodate the SYM53C720's wide SCSI data transfer capability. The register is utilized during synchronous and asynchronous data send.

Benefit

The addition of these bits makes the SYM53C720 to send 16 bits of data at a time.

SCSI Bus Data Lines Bits

Function

Bits 15 through 8 in the SCSI Bus Data Lines Register were added to allow the extra data bits on the SCSI bus to be read. This data is not latched and may be changing while being read.

Benefit

The addition of these bits makes it possible to look at all the SCSI data lines at once.

SCRATCH Register One

Function

The SCRATCH register is a second general purpose user definable 32-bit read/write register.

Benefit

The SCRATCH register is used as a general purpose holding register.