SYM53C700 AND SYM53C710 COMPARISON

Introduction

This engineering note compares the SYM53C710 with the SYM53C700. There are four categories of SYM53C710 differences: register, host bus interface, SCRIPTS Instruction, and SCSI bus. The "Features" section summarizes the high-level differences.

A. FEATURES

	SYM53C700	SYM53C710
1. SCSI Data Transfer Rate		
− Asynchronous	5 Mbytes/sec	5 Mbytes/sec
− Synchronous	6.25 Mbytes/sec	10 Mbytes/sec
2. DMA Data Transfer Rate	50 Mbytes/sec	132 Mbytes/sec
3. Byte Orientation	Little Endian	Big or Little Endian
4. Host Bus Multiplexing	N/A	Optional
5. Host Bus Width	16 or 32 bits	32 bits only
6. SCSI Watchdog Timer	N/A	Available
7. Separate SCSI Clock	N/A	Available
8. Glitchless SCSI on Power Up/Down	N/A	Available
9. Dynamic Altering of SCRIPTs	Patching Required	Table Indirect Data Mode
10. Loading SCRIPTs Into PROMs	N/A	Relative Jump and Table Indirect Modes
11. DMA Controller	N/A	Memory to Memory Move Instruction
12. Dynamic Altering of Registers	N/A	Register Read/Write Instruction
13. Multi-threaded I/O	Supported	Advanced - Memory to Memory Move and Register Read/Write Instructions - Relative Jump and Table Indirect Modes
14. Number of Interrupts	1 per disconnect	1 per I/O

B. <u>REGISTER DIFFERENCES</u>

Figure B-1 summarizes the differences between the SYM53C700 and the SYM53C710 register sets. The register/bit additions and the resulting benefits to the user are described below. For a more detailed explanation of each of the registers in the SYM53C710, reference the SYM53C710 Data Manual.

1. Synchronous SCSI Clock Control Bits.

    Function: Two bits within the SBCL register have been added to allow modification of the synchronous SCSI clock with respect to SCLK. These bits allow the synchronous logic within the chip to run at a different speed from the asynchronous logic.

    Benefit: This addition allows for optimal utilization of Fast SCSI -2.

2. Bus Fault Bit.

    Function: This bit has been added to the DSTAT register and is set when a bus fault condition has been detected.

    Benefit: SCRIPTS software may use this bit to determine if an interrupt was caused by a bus fault.

3. Data Structure Address Register.

    Function: The DSA register has been added to enable implementation of the Table Indirect SCRIPTS addressing mode. The value stored in the DSA register is the base address to be used for Table Indirect calculations. The Table Indirect SCRIPTS addressing mode is described in detail in the SYM53C710 Programmer's Guide.

    Benefit: The Table Indirect addressing mode allows the separation of data structures from SCRIPTS instructions. With this capability, no dynamic altering of the SCRIPTs instructions is required at start I/O, and all of the code may be placed on a PROM.

4. Signal Process Test and Reset Bit.

    Function: The SIGP bit has been added as a flag which may be passed to or from a running SCRIPT. The only SCRIPTS instruction directly affected by the SIGP bit is Wait for Selection/Reselection. The SIGP bit exists in both the CTEST2 and ISTAT registers. Since a SCRIPTS driver can only access the ISTAT register, it reads and writes the SIGP bit in the ISTAT register. Reading the CTEST2 register clears the bit.

    Benefit: The SIGP bit provides the user with additional flexibility in setting and reading a user-defined flag while running a SCRIPTs program. Furthermore, in an infinite Wait for Selection/Reselection situation, the SIGP bit causes the SYM53C710 to jump to an alternate address. The SYM53C700 must be aborted in this situation.

Figure B-1. Register/Bit Differences

NEW

ITEM	SYM53C700	SYM53C710
Data Structure Address Register	n/a	DSA
CTEST8 Register	n/a	CTEST8
LCRC Register	n/a	LCRC
Scratch Register	n/a	SCRATCH
Adder Output Register	n/a	ADDER
Synchronous SCSI Clock Control Bits	n/a	SBCL, bits 1-0
Bus Fault Bit	n/a	DSTAT, bit 5
SIGnal Process Test & Reset Bit	n/a	CTEST2, bit 6
MUX Mode Bit	n/a	CTEST4, bit 7
Cache Burst Disable Bit	n/a	CTEST7, bit 7
Snoop Control Bits 1-0	n/a	CEST7, bits 6-5
Transfer Type One Bit	n/a	CEST7, bit 1
Byte Offset Six Bit	n/a	DFIFO, bit 6
SIGnal Process Set Bit	n/a	ISTAT, bit 5
FETCH/ Pin Control Bit	n/a	CTEST8, bit 1
Snoop Mode Bit	n/a	CTEST8, bit 0
Function Code Bits 2-1	n/a	DMODE, bits 5-4
Program/Data Function Code 0 Control Bit	n/a	DMODE, bit 3
UPSO-TTO/ Bit	n/a	DMODE, bit 1
Bus Fault Interrupt Enable Bit	n/a	DIEN, bit 5
Enable Acknowledge Control Bit	n/a	DCNTL, bit 5
Fast Arbitration Mode Bit	n/a	DCNTL, bit 1
SYM53C700 Compatibility Bit	n/a	DCNTL, bit 0

DELETED

ITEM	SYM53C700	SYM53C710
DC/ Pin Control Bit	CTEST7, bit 1	n/a
DSPS and DSP Empty Bit	ISTAT, bit 2	n/a
16-Bit DMA, '286-Mode Bits	DMODE, bits 5-4	n/a
I/O - Memory Mapped DMA Bit	DMODE, bit 3	n/a
Pipeline Mode Bit	DMODE, bit 1	n/a
16-Bit SCSI Scripts Mode Bit	DCNTL, bit 5	n/a
Real Target Mode Bit	CTEST0, bit 1	n/a

MOVED

ITEM	SYM53C700	SYM53C710
Flush FIFO bit	DFIFO, bit 7	CTEST8, bit 3
Clear FIFO bit	DFIFO, bit 6	CTEST8, bit 2
Software Reset Bit	DCNTL, bit 0	ISTAT, bit 6
Chip Revision Level Bits	CTEST7, bits 7-4	CTEST8, bits 7-4
DMODE Register	Address 34h	Address 38h

5. MUX Mode Bit.

    Function: The MUX Mode bit was added to allow the data and address busses of the SYM53C710 to be tied together. In this mode, as bus master, the SYM53C710 will assert an address and then send or receive data over a common 32 bit bus.

    Benefit: The MUX Mode bit allows the SYM53C710 to operate without external hardware on those host busses on which data and addresses share a common 32 bit bus. Sbus is an example of a multiplexed bus.

6. Cache Burst Disable Bit.

    Function: The CDIS bit disables Cache-Line Burst mode. When this bit is clear, the chip will attempt Cache-Line bursts when two conditions are met. The first condition is that the address must be lined up to a cache line boundary (A3-A0 must be 0). The second condition is that the transfer counter must be greater than 32. Cache-Line Burst mode eliminates the need for a full handshake between the bus master and the memory device when transferring data.

    Benefit: Cache-Line Burst mode allows up to 66 Mbytes/sec DMA burst bandwidth for extremely high data transfer rates.

7. Snoop Control Bits.

    Function: The SC0 and SC1 bits control the two Snoop Control pins. The SC1 bit controls the Snoop Control 1 pin all of the time. The SC0 bit controls the Snoop Control 0 pin only when the Snoop Mode bit is not set. Monitoring the SC0 bit gives advance notice of a pending SYM53C710 bus request. Bus snooping allows for transmission of additional information to other devices on the host bus about the current type of transfer.

    Benefit: The addition of the Snoop Control bits/pins allow the 68040 host processor to snoop an alternate master read/write transfer, ensuring access to valid data. In a non-68040 environment, these bits/pins provide additional user-defined functionality.

8. Transfer Type One Bit.

    Function: The TT1 bit controls the Transfer Type 1 output pin. It is a user-controlled output bit which is asserted during bus master cycles. This signal is snooped by other devices to determine the type of transfer.

    Benefit: The TT1 bit/pin allows the 68040 host processor to snoop the transfer. In a non-68040 environment, this bit/pin provides additional user-defined functionality.

9. Byte Offset Six Bit.

    Function: This bit is now the most significant bit of the DMA FIFO byte offset counter. The byte offset counter has been increased by one bit to account for the DMA FIFO doubling in size. The DMA FIFO in the SYM53C710 is 64 bytes, whereas it is 32 bytes in the SYM53C700.

    Benefit: A larger DMA FIFO allows for more efficient speed matching between SCSI and host busses.

10. FETCH Pin Control Bit.

Function: The FM bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH allows direct access to SCRIPTS instructions residing in local memory.

Benefit. FETCH can alleviate the long delay associated with arbitrating for the host bus in order to fetch SCRIPTS instructions from system memory by allowing SCRIPTS to reside in local memory.

11. Snoop Mode Bit.

Function: The SM bit causes the snoop mode pins to become active either during all cycles or only during a bus master cycle. The Snoop Control 1 pin will be controlled by SC1 in the CTEST7 register. Depending on the SM bit, the Snoop Control 0 pin will either be controlled by SC0 in the CETEST7 register or become a copy of the internal bus request signal. The Snoop Control 0 signal will assert prior to BR/ and will be negated during the AS/ of the last bus cycle.

Benefit. The 68040 host processor may snoop to alternate master read/write transfer, ensuring access to valid data. In an non-68040 environment, these bits/pins provide additional user-defined functionality.

12. Longitudinal Parity Register.

Function: The primary function of the LCRC register is to accumulate an exclusive or of all data that is transferred between the DMA FIFO and the SCSI core. Also, like the SFBR register in the SYM53C700, the LCRC register is used by the SCSI core to hold the SCSI ID value during selection and reselection. This register should be used instead of the SFBR register because the SFBR is used as an accumulator during many SCRIPTS operations and may be overwritten at any time.

Benefit: The LCRC register ensures correct data transfer and alleviates the problem of the SFBR register being overwritten during SCRIPTS operations.

13. SCRATCH Register.

Function: The SCRATCH register is a general purpose user definable 32 bit read/write register.

Benefit. The SCRATCH register combined with register to register move, AND, OR, and ADD operations provides the capability to write a complete SCSI interface program in SCRIPTS.

14. Function Code and Program/Data Function Code 0 Control Bits.

Function: FC1 and FC2 in the DMODE register control the Function Code 1 and 2 output pins. The PD bit within the DMA Mode register controls the Function Code 0 output pin. These are user-controlled pins which will be active during bus master cycles. The bus master specifies a target address space for every bus cycle with the function code signals according to the type of access required. In addition to distinguishing between supervisor/user and program/data, the bus master can identify special processor cycles, such as the interrupt acknowledge cycle, and the memory management unit can control accesses and translate addresses appropriately.

Benefit: The Function Code bits/pins correspond to functions available in the 680X0 family. In a non-680X0 environment, these bits/pins provide additional user-defined functionality.

15. User Programmable Transfer Type Bit.

Function: The UPSO/TT0 controls the UPSO-TT0/ general purpose output pin. This bit is asserted while the SYM53C710 is a bus master to indicate the type of access for the current bus transfer.

Benefit: The UPS0/TT0 bit/pin corresponds to a 68040 signal. In a non-68040 environment, these bits/pins provide additional user-defined functionality.

16. Bus Fault Interrupt Enable Bit.

Function: Assertion of this bit enables a bus fault to generate a hardware interrupt.

Benefit: This bit allows additional control of SYM53C710 operations.

17. Enable Acknowledge Control Bit.

Function: Assertion of the EA bit within the DCNTL register causes the STERM/-TA pin to become bi-directional. As a result, the SYM53C710 will generate STERM/-TA during slave accesses. The SLACK/ and STERM/ pins in the SYM53C710 correspond to the READYO/ and READYI/ pins in the SYM53C700.

Benefit: The EA bit reduces the amount of logic required to interface with a different bus.

18. Fast Arbitration Mode Bit.

Function: Assertion of the FA bit within the DCNTL register allows the SYM53C710 to immediately become bus master after receiving a bus grant. In arbitration mode the SYM53C710 bypasses the GRANT cycle and moves directly from the REQUEST to the START cycle.

Benefit: The SYM53C710 starts driving addresses sooner than the SYM53C700; some busses, i.e. EISA, expect immediate assertion of valid address lines.

19. SYM53C700 Compatibility Bit.

Function: The COM bit within the DCNTL register allows the SYM53C710 to behave in a manner compatible with the SYM53C700. Selection/reselection IDs are stored in both the LCRC and SFBR registers, and auto switching is enabled.

Benefit: This bit provides compatibility between SYM53C700 software and the SYM53C710 chip.

20. Adder Output Register.

Function: This is a read-only register which contains the 32 bit output of the internal adder.

Benefit: The Adder Output register allows the SYM53C710 to perform ADD, AND, and OR and "relative" calculations.

C. HOST BUS INTERFACE DIFFERENCES

The SYM53C710 host bus interface has been significantly enhanced over that of the SYM53C700. Greater flexibility and functionality has been provided allowing the SYM53C710 to directly interface with a larger number of host busses. The SYM53C710 host bus interface differences are as follows:

1. Cache-Line Burst:

Function: Cache-Line Burst mode eliminates the need for a full handshake between the bus master and the memory device when transferring data. The bus master will arbitrate at the beginning of each 16 byte data transfer and is able to transfer 4 bytes per clock second.

Benefit: Cache-Line Burst mode allows up to 66 Mbytes/sec DMA burst bandwidth for extremely high data transfer rates or data streaming modes. The SYM53C700 is only capable of 50 Mbytes/sec DMA transfers.

2. Big/Little Endian.

Function: Big/Little Endian mode allows the SYM53C710 to adjust to specific byte orientations. This mode is controlled by the BIG_LIT/ pin. Big Endian is the byte ordering scheme adopted by Motorola for use with their processors; Little Endian is the byte ordering scheme adopted by Intel for use with their processors. Internally, the byte lanes of the DMA FIFO and registers are not modified with respect to D31-D0 and are physically arranged in Little Endian order. The SYM53C710 will adjust the byte control logic of the DMA FIFO and register decodes to enable the appropriate byte lane for the current operating mode. The registers will always appear in the same byte lane, but the address of the register will be repositioned. When a long word is accessed, no repositioning of the byte wide data is required in either mode. Since long word accesses are always used to fetch SCRIPTS, programming compatibility will be maintained.

Big Endian Mode: The sequencers within the SYM53C710 will transfer D31-D24 as the first bye out of the FIFO, D23-D16 as the second byte, etc. The register addresses will be mapped so that the lowest physical address will appear in D31-D24.

Big Endian Byte Access Table

System Data Bus	D31-D24	D23-D16	D15-D8	D7-D0
SYM53C710 Pins	D31-D24	D23-D16	D15-D8	D7-D0
Register	SIEN	SDID	SCNTL1	SCNTL0
Address	00h	01h	02h	03h

Little Endian Mode: The sequencers within the SYM53C710 will transfer D7-D0 as the first byte out of the FIFO, D15-D8 as the second byte, etc. The register addresses will be mapped so that the lowest physical address will appear in D7-D0.

Little Endian Byte Access Table

System Data Bus	D31-D24	D23-D16	D15-D8	D7-D0
SYM53C710 Pins	D31-D24	D23-D16	D15-D8	D7-D0
Register	SIEN	SDID	SCNTL1	SCNTL0
Address	03h	02h	01h	00h

Benefit: The Big/Little Endian pin allows the SYM53C710 to be interfaced to any system with little, if any, additional hardware required.

3. BACK-OFF.

Function: When a higher priority bus master requires access to the bus, it notifies the SYM53C710 through the BACK-OFF pin. When this signal is asserted, the SYM53C710 will finish the current cycle before releasing control of the bus. The SYM53C710 will not try to arbitrate for the bus until this signal is reset.

Benefit: Through the use of the BACK-OFF pin, the system may preempt the SYM53C710 to allow a higher priority device to control the bus.

4. Bus Retry.

Function: Bus Retry is similar to BACK-OFF in that it allows a higher priority device access to the bus. There are two differences between BACK-OFF and Bus Retry. The first difference is that with a Bus Retry the SYM53C710 will immediately relinquish control of the bus without finishing the current cycle. The second difference is that after releasing the bus due to a Bus Retry, the SYM53C710 will immediately try to arbitrate for the host bus.

Benefit: Bus Retry allows the CPU to remove the SYM53C710 from the bus to resolve bus deadlocks and eliminate system hardware lock-ups.

5. Fast Arbitration.

Function: Fast Arbitration mode removes one clock cycle from the host bus arbitration time. The Fast Arbitration Mode bit within the DCNTL register controls this mode.

Benefit: Fast Arbitration mode allows the SYM53C710 to function on host busses, such as EISA, which expect immediate assertion of address lines. In this mode the SYM53C710 may also more efficiently utilize bus bandwidth.

6. FETCH.

Function: FETCH allows the SYM53C710 to directly access SCRIPTS instructions from local memory. Implementation of this capability is controlled by the FETCH/ Pin Control Bit in the CTEST8 register.

Benefit: FETCH provides faster SCRIPTS execution especially in systems which have a large bus latency for arbitration. FETCH also provides the user with more control over the configuration of the system and allows for "far memory" applications.

7. Host Bus Multiplex.

Function: Host bus multiplexing allows the SYM53C710 to tie the address and data lines together. In this mode, as bus master, the SYM53C710 will assert an address and then send or receive data over a common 32 bit bus. This function is controlled via the MUX bit within the CTEST4 register.

Benefit: Multiplexing allows the SYM53C710 to operate without external hardware on those busses on which data and addresses share a common 32 bit bus. SBus is an example of this type of bus.

8. Host Bus Operating Mode.

Function: The SYM53C710 is capable of interfacing with host busses in both synchronous and asynchronous modes, whereas the SYM53C700 is only capable of interfacing in synchronous mode without additional external hardware.

Benefit: The ability to interface with a host bus in asynchronous mode provides the user with additional flexibility.

D. **SCRIPTS INSTRUCTION DIFFERENCES**

Two SCRIPTS instructions have been added to the SYM53C710. Since the SYM53C710 still utilizes all of the SCRIPTS instructions which were available with the SYM53C700, SCRIPTS programs developed for a SYM53C700 will be upward compatible. For a more detailed description of the SCRIPTS language, reference the SYM53C710 Programmer's Guide.

1. Table Indirect.

   Function: Table Indirect Data Mode allows the SYM53C710 to execute I/O data structures. The SCRIPTS contains the table offset that is combined with the base address stored in the DSA register to generate the 32 bit address from which to fetch byte counts, data buffer addresses, etc. With this feature, data structures are separated from SCRIPTS instructions.

   Benefit: The Table Indirect Data Mode allows for all of the SCRIPTS code to be placed in a PROM since no dynamic altering of SCRIPTS instructions would be required at start I/O.

2. Relative Jump.

   Function: Relative Jump mode allows for jumps within a SCRIPTS program for an offset address forward or backward.

   Benefit: The Relative Jump feature allows a SCRIPTS program to be loaded into system memory with no patching of the code required and is one of the requirements for loading a SCRIPTS program into a PROM. Complexity of the power up firmware is reduced by this feature.

3. Memory to Memory Move.

   Function: The Memory to Memory Move instruction allows the SYM53C710 as bus master to move data within system memory.

   Benefit: The Memory to Memory Move instruction allows the programmer to use the SYM53C710 as a high performance (40 Mbytes/sec) DMA controller. Mass data movements can be accomplished with no system processor intervention. This feature also allows the user to save state upon a disconnect and resume automatically upon reselect with no processor intervention.

4. Register Read/Write.

   Function: The Register Read/Write instruction allows the SYM53C710 to write and read its own registers.

   Benefit: Writing the SYM53C710 registers from a SCRIPT allows the user to completely configure the chip from SCRIPTS and to check status or alter synchronous offset and period dynamically with no requirement for an external processor.

E. SCSI BUS INTERFACE DIFFERENCES

The SCSI bus interface of the SYM53C710 is not significantly different FROM that of the SYM53C700. The primary difference is the implementation of Fast SCSI. The SYM53C710 differences are as follows:

1. Fast SCSI

    Function: The SYM53C710 transfers data over the SCSI bus at 10 Mbytes/sec whereas the SYM53C700 does it at 6.25 Mbytes/sec. This applies only when the SCSI bus is operating in synchronous and differential modes.

    Benefit: Fast SCSI provides a significant increase in system performance especially in systems requiring a large amount of data transfer between host and peripheral devices.

2. Separate SCSI clock.

    Function: The SYM53C710 has a separate SCSI clock which operates at up to 50 MHz. The SYM53C700 derives SCSI timings from the bus clock which tends to be considerably slower.

    Benefit: Separate SCSI and bus clocks allow the host interface to operate at a lower speed while a higher speed clock controlling the SCSI bus guarantees Fast SCSI timings of 10 Mbytes/sec.

3. SCSI Watchdog Timer.

    Function: A watchdog timer will, if activated, interrupt the SYM53C710 when it detects 250 msec. of no activity over the bus.

    Benefit: The watchdog timer within the SYM53C710 is provided so that the system does not have to furnish it.