Testability of the SYM53C90 Family of SCSI Controllers

The SYM53C90 Family of SCSI controllers includes the following chips: SYM53C90, SYM53C90A, SYM53C90B, SYM53C94 and SYM53C95.

Test Register (Address 0Ah, write only)

The SYM53C90 has a test register which can be used to test the functionality of the chip. The test register allows the user to place the chip in Target mode, Initiator mode, and Tri-state mode. The test mode bit of the Configuration Register (Address 8, bit 3) must be set before writing any of the Test Register bits.

- Bit 0 - Target Mode

When this bit is set, the chip will be placed in the target mode, and the TGS output will be asserted regardless of the state of the DIFFM input. BSYO/, REQO/, IOO/, CDO/, and MSGO/ will not be asserted on the SCSI bus until a target command is issued. For example, when a Send Data command is issued (22h), BSYO/, REQO/, and IOO/ will be asserted. Any target mode commands can be used to test each of the control lines asserted by a target device. The illegal command interrupt can also be tested by issuing commands other than target mode commands.

- Bit 1 - Initiator Mode

When this bit is set, the chip will be placed in the initiator mode, but the IGS output will not be asserted immediately. None of the initiator commands will function until one of the Select commands has been issued. Once a Select command is completed, the initiator commands will function properly. After issuing a Select command, the IGS output is asserted at the same time as the SELO/ signal.

- Bit 2 - Tri-State Mode

When this bit is set, all outputs will be tri-stated.

- Bits 3-7 - Presently these bits are unused and should not be set (1).

Basic Functionality Tests

The following describes some simple tests that can be used to check the chip's functionality.

- Load the FIFO with data bytes and read them back to verify the FIFO operation. The FIFO Flags Register (Address 7) can be used to verify how many bytes were written to the FIFO.
- Load the Transfer Count Registers (Write-only Addresses 0 & 1), and issue a DMA NOP command (80h). The value written to the Transfer Count Registers will be loaded into the Transfer Counter Registers (Read-only Addresses 0 & 1) any time a command is issued with DMA enabled (Bit 7=1 of the command register).
- Write to the Configuration Register and make sure that you can read the same value back.
- When the chip is in a disconnected state, issue an initiator or target command. This should cause an illegal command interrupt (Bit 6=1 of the Interrupt Status Register).
- When no other SCSI devices are connected to the SCSI bus, the Selection/Reselection timeout and the assertion of each data bit can be tested. A test that tries to select each SCSI ID will check to see that each SCSI data line is asserted. Since there are no other SCSI devices currently connected on the bus, the selection timeout function can also be tested in this manner.
- The Parity Test mode can also be used to force bad parity on the SCSI bus to evaluate how another device handles parity errors. The Parity Test mode is enabled by writing a 1 to bit 5 of the Configuration Register (Address 8).

DMA Operational Tests

The following describes how to check the functionality of the DMA channel.

DMA Transfers to the SYM53C90 (DMA Write)

1) Reset the chip by either asserting the RESET input, or by issuing a Reset Chip command.
2) If a Reset Chip command was issued to any SYM53C90 chip (SYM53C90, SYM53C90A, SYM53C90B, SYM53C94, SYM53C95) then a NOP must be the next command issued to the chip before writing to any other register.
3) Set bit 3 of the Configuration Register (Address 8) to enable the test mode.
4) Set bit 0 of the Test Register (Address A) to put the chip into the target test mode.
5) Load the Transfer Count Registers (Addresses 0 & 1) with the number of bytes to transfer. If you load the transfer counter with a value greater than the number of bytes to be transferred, the DREQ output will remain asserted until the transfer counter has decremented to zero.
6) Issue a Send Data w/DMA command (A2h).
7) Wait ~1æs to allow plenty of time for internal command synchronization and bus settle delays. The chip will assert the DREQ output and the SCSI phase lines to the Data In phase.

8) Wait whatever additional time required to guarantee that your DMA controller has transferred the desired number of bytes to the SCSI chip.

9) The first byte received by the SCSI chip from the DMA controller is automatically unloaded from the FIFO and asserted on the SCSI bus. The remaining bytes may be verified by reading the FIFO Flags Register and the FIFO register.

10) Reset the chip or reset the SCSI bus to release all SCSI signals.

DMA Transfers from the SYM53C90 (DMA Read)

1) Reset the chip by either asserting the RESET input, or by issuing a Reset Chip command.

2) If a Reset Chip command was issued to any SYM53C90 chip (SYM53C90, SYM53C90A, SYM53C90B, SYM53C94, SYM53C95) then a NOP must be the next command issued to the chip before writing to any other register.

3) Set bit 3 in the Configuration Register (Address 8) to enable the test mode.

4) Set bit 0 of the Test Register (Address A) to put the chip into the target test mode.

5) Load the Transfer Count Registers (Addresses 0 & 1) with the number of bytes to transfer. If you load the transfer counter with a value greater than the number of bytes to be transferred, the DREQ output will remain asserted until the transfer counter has decremented to zero.

6) Issue a Receive Data w/DMA command (AAh).

7) Wait ~1æs to allow plenty of time for internal command synchronization and bus settle delays. The chip will assert the DREQ output and the SCSI phase lines to the Data Out phase.

8) Wait whatever additional time required to guarantee that your DMA controller has transferred the desired number of bytes from the SCSI chip.

9) The data loaded into the FIFO can be compared to the data written to memory by the DMA controller.

10) Reset the chip or reset the SCSI bus to release all SCSI signals.